

Service Manual KF300





lodel : KF30

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1. INTRODUCTION

1.1 Purpose

This manual provides the information necessary to repair, calibration, description and download the features of this model.

1.2 Regulatory Information

A. Security

Toll fraud, the unauthorized use of telecommunications system by an unauthorized part (for example, persons other than your company's employees, agents, subcontractors, or person working on your company's behalf) can result in substantial additional charges for your telecommunications services. System users are responsible for the security of own system. There are may be risks of toll fraud associated with your telecommunications system. System users are responsible for programming and configuring the equipment to prevent unauthorized use. The manufacturer does not warrant that this product is immune from the above case but will prevent unauthorized use of common-carrier telecommunication service of facilities accessed through or connected to it.

The manufacturer will not be responsible for any charges that result from such unauthorized use.

B. Incidence of Harm

If a telephone company determines that the equipment provided to customer is faulty and possibly causing harm or interruption in service to the telephone network, it should disconnect telephone service until repair can be done. A telephone company may temporarily disconnect service as long as repair is not done.

C. Changes in Service

A local telephone company may make changes in its communications facilities or procedure. If these changes could reasonably be expected to affect the use of the this phone or compatibility with the network, the telephone company is required to give advanced written notice to the user, allowing the user to take appropriate steps to maintain telephone service.

D. Maintenance Limitations

Maintenance limitations on this model must be performed only by the manufacturer or its authorized agent.

The user may not make any changes and/or repairs expect as specifically noted in this manual. Therefore, note that unauthorized alternations or repair may affect the regulatory status of the system and may void any remaining warranty.

1. INTRODUCTION

E. Notice of Radiated Emissions

This model complies with rules regarding radiation and radio frequency emission as defined by local regulatory agencies. In accordance with these agencies, you may be required to provide information such as the following to the end user.

F. Pictures

The pictures in this manual are for illustrative purposes only; your actual hardware may look slightly different.

G. Interference and Attenuation

Phone may interfere with sensitive laboratory equipment, medical equipment, etc.Interference from unsuppressed engines or electric motors may cause problems.

H. Electrostatic Sensitive Devices

ATTENTION

Boards, which contain Electrostatic Sensitive Device (ESD), are indicated $\stackrel{\frown}{\bigotimes}$ by the sign. Following information is ESD handling:

- Service personnel should ground themselves by using a wrist strap when exchange system boards.
- When repairs are made to a system board, they should spread the floor with anti-static matb which is also grounded.
- · Use a suitable, grounded soldering iron.
- Keep sensitive parts in these protective packages until these are used.
- When returning system boards or parts like EEPROM to the factory, use the protective package as described.

1.3 Abbreviations

For the purposes of this manual, following abbreviations apply:

APC	Automatic Power Control	
ВВ	Baseband	
BER	Bit Error Ratio	
CC-CV	Constant Current - Constant Voltage	
DAC	Digital to Analog Converter	
DCS	Digital Communication System	
dBm	dB relative to 1 milli watt	
DSP	Digital Signal Processing	
EEPROM	Electrical Erasable Programmable Read-Only Memory	
ESD Electrostatic Discharge		
FPCB Flexible Printed Circuit Board		
GMSK Gaussian Minimum Shift Keying		
GPIB General Purpose Interface Bus		
GSM	Global System for Mobile Communications	
IPUI	International Portable User Identity	
IF	Intermediate Frequency	
LCD Liquid Crystal Display		
LDO	Low Drop Output	
LED	Light Emitting Diode	
OPLL	Offset Phase Locked Loop	

1. INTRODUCTION

PAM	Power Amplifier Module
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
PLL	Phase Locked Loop
PSTN	Public Switched Telephone Network
RF	Radio Frequency
RLR	Receiving Loudness Rating
RMS	Root Mean Square
RTC	Real Time Clock
SAW	Surface Acoustic Wave
SIM	Subscriber Identity Module
SLR	Sending Loudness Rating
SRAM	Static Random Access Memory
PSRAM	Pseudo SRAM
STMR	Side Tone Masking Rating
TA	Travel Adapter
TDD	Time Division Duplex
TDMA	Time Division Multiple Access
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator
VCTCXO	Voltage Control Temperature Compensated Crystal Oscillator
WAP	Wireless Application Protocol

2. SYSTEM SPECIFICATION

2.1 H/W Features

Item	Feature	Comment
Standard Battery	Li-ion Polymer, 3.7V 800mAh	
Stand by TIME	Up to 200 hrs : Paging Period 5, RSSI 85dBm	
Talk time	Up to 200min : GSM Tx Level 7	
Stand by time	Up to 200 hours (Paging Period: 5, RSSI: -85 dBm)	
Charging time	Approx. 3 hours	
RX Sensitivity	GSM850/EGSM: -109dBm, DCS/PCS: -109dBm	
TX output power	GSM850, EGSM: 32.4dBm(Level 5), DCS , PCS: 29.5dBm(Level 0)	
GPRS compatibility	Class 10	
SIM card type	3V Small	
Dioplay	MAIN: TFT 240 × 320 pixel 262K Color	
Display	SUB : TFT 128 × 160 pixel 262K Color	
Status Indicator	Hard icons. Key Pad 0 ~ 9, #, *, Up/Down/Left/Right/Ok Navigation Key Menu Key, Clear Key, Back Key, Confirm Key Send Key, Volume Key, PWR Key, Camera Key, Hot Key	
ANT	Internal	
EAR Phone Jack	Yes	
PC Synchronization	Yes	
Speech coding	EFR/FR/HR	
Data and Fax	Yes	
Vibrator	Yes	
Loud Speaker	Yes	
Voice Recoding	Yes	
Microphone	Yes	
Speaker/Receiver	16Ø Speaker / 11x07 Receiver	
Travel Adapter	Yes	
MIDI	SW MIDI (Mono SPK)	
Camera	2M	
Bluetooth / FM Radio	Bluetooth version 2.0 / 76~108MHz supported	

2.2 Technical Specification

Item	Description	Specification					
1	Frequency Band	GSM850 • TX: 824 ~ 849MHz • RX: 869 ~ 894MHz EGSM • TX: 880 ~ 915MHz • RX: 925 ~ 960MHz DCS1800 • TX: 1710 ~ 1785MHz					
		PCS19	1805 ~ 1886 900 1850 ~ 1910 1930 ~ 1990)MHz			
2	Phase Error		5 degrees < 20 degrees	s			
3	Frequency Error	< 0.1 p	pm				
		GSM8	50/EGSM				
		Level	Power	Toler.	Level	Power	Toler.
		5	33 dBm	±2dB	13	17 dBm	±3dB
		6	31 dBm	±3dB	14	15 dBm	±3dB
		7	29 dBm	±3dB	15	13 dBm	±3dB
		8	27 dBm	±3dB	16	11 dBm	±5dB
		9	25 dBm	±3dB	17	9 dBm	±5dB
		10	23 dBm	±3dB	18	7 dBm	±5dB
		11	21 dBm	±3dB	19	5 dBm	±5dB
4	Power Level	12	19 dBm	±3dB			
		DCS/P	CS				
		Level	Power	Toler.	Level	Power	Toler.
		0	30 dBm	±2dB	8	14 dBm	±3dB
		1	28 dBm	±3dB	9	12 dBm	±4dB
		2	26 dBm	±3dB	10	10 dBm	±4dB
		3	24 dBm	±3dB	11	8 dBm	±4dB
		4	22 dBm	±3dB	12	6 dBm	±4dB
		5	20 dBm	±3dB	13	4 dBm	±4dB
		6	18 dBm	±3dB	14	2 dBm	±5dB
		7	16 dBm	±3dB	15	0 dBm	±5dB

Item	Description	Specification			
		GSM850/EGSM			
		Offset from Carrier (kHz).	Max. [dBc]		
		100	0.5		
		200	-30		
		250	-33		
		400	-60		
		600 ~ 1,200	-60		
		1,200 ~ 1,800	-60		
		1,800 ~ 3,000	-63		
		3,000 ~ 6,000	-65		
5	Output RF Spectrum	6,000	-71		
5	(due to modulation)	DCS/PCS			
		Offset from Carrier (kHz).	Max. [dBc]		
		100	0.5		
		200	-30		
		250	-33		
		400	-60		
		600 ~ 1,200	-60		
		1,200 ~ 1,800	-60		
		1,800 ~ 3,000	-65		
		3,000 ~ 6,000	-65		
		6,000	-73		
		GSM850/EGSM			
		Offset from Carrier (kHz)	Max. [dBm]		
6	Output RF Spectrum	400	-19		
	(due to switching transient)	600	-21		
		1,200	-21		
		1,800	-24		

2. SYSTEM SPECIFICATION

Item	Description	Specification			
		DCS/PCS			
		Offset from Carrier (kHz)		Max. [dBm]	
	Output RF Spectrum	400			-22
6	(due to switching transient)	600			-24
		1,200			-24
		1,800			-27
7	Spurious Emissions	Conduction, Emission Status	1		
8	Bit Error Ratio	GSM850/EGSM BER (Class II) < 2.439% @-102 dBm DCS/PCS BER (Class II) < 2.439% @-100 dBm			
9	RX Level Report Accuracy	±3 dB			
10	SLR	8 ±3 dB			
		Frequency (Hz)	Max.(d	B)	Min.(dB)
		100	-12		-
		200	0		-
		300	0		-12
11	Sending Response	1,000	0		-6
		2,000	4		-6
		3,000	4		-6
		3,400	4		-9
		4,000	0		-
12	RLR	2 ±3 dB			
		Frequency (Hz)	Max.(d	B)	Min.(dB)
		100	-12		-
		200	0		-
	Receiving Response	300	0		-12
13		1,000	0		-6
		3,000	4		-6
		3,400	4		-6
		4,000	4		-9
		*Mean that Adopt a straight lir			0 Hz
		and 1,000 Hz to be Max. level	in the ran	ge.	

14 STMR 13±5 dB 15 Stability Margin > 6 dB 16 Distortion dB to ARL (dB) Level Ratio (dB) -35 17.5 -30 22.5 -20 30.7 -10 33.3 0 33.7 7 31.7 10 25.5 17 Side Tone Distortion Three stage distortion < 10% System frequency (13 MHz) tolerance ≤ 2.5 ppm 19 32.768KHz tolerance ≤ 30 ppm At least 65 dBspl under below conditions: 1. Ringer set as ringer. 2. Test distance set as 50 cm Past Charge: Typ. 430 mA Slow Charge: Typ. 80mA Total Charging Time : < 3 hours Bar Number Power 7 → 5 -93 ± 2 Antenna Display 5 → 4 -98 ± 2 4 → 2 -101 ± 2 2 → 1 -104 ± 2 1 → 0 -106 ± 2 0 → OFF ~106 Battery Bar Number Voltage 3 ≤ 3.75 ± 0.05 V	Item	Description	Specification			
Ab to ARL (dB) Level Ratio (dB)	14	STMR	13 ±5 dB			
16 Distortion	15	Stability Margin	> 6 dB			
16 Distortion -30 22.5			dB to ARL (dB)	Level Ratio (dB)		
Distortion			-35	17.5		
16			-30	22.5		
-10 33.3 0 33.7 7 31.7 10 25.5 17 Side Tone Distortion Three stage distortion < 10% System frequency (13 MHz) tolerance ≤ 2.5 ppm 4 t least 65 dBspl under below conditions: 1. Ringer set as ringer. 2. Test distance set as 50 cm 21 Charge Current Fast Charge : Typ. 430 mA Slow Charge : Typ. 80mA Total Charging Time : < 3 hours Bar Number Power 7 93~ 7→5 93±2 5→4 98±2 4→2 -101±2 2→1 -104±2 1→0 -106±2 0→OFF ~106 Battery Bar Number Voltage 3 ≤3.75±0.05 V	16	Distortion	-20	30.7		
7 31.7 10 25.5 17 Side Tone Distortion Three stage distortion < 10%		Distortion	-10	33.3		
10 25.5 17 Side Tone Distortion Three stage distortion < 10% System frequency (13 MHz) tolerance ≤ 2.5 ppm 20 Ringer Volume At least 65 dBspl under below conditions: 1. Ringer set as ringer. 2. Test distance set as 50 cm Past Charge: Typ. 430 mA Slow Charge: Typ. 80mA Total Charging Time: < 3 hours Bar Number Power 7 -93~ 7→5 -93 ± 2 22 Antenna Display 5→4 -98 ± 2 4→2 -101 ± 2 2→1 -104 ± 2 1→0 -106 ± 2 0→OFF ~106 Battery Bar Number Voltage 3 ≤ 3.75 ± 0.05 V 23 Battery Indicator 3→2 3.75 ± 0.05 V			0	33.7		
17 Side Tone Distortion Three stage distortion < 10% 18 System frequency (13 MHz) tolerance ≤ 2.5 ppm 19 32.768KHz tolerance ≤ 30 ppm 20 Ringer Volume At least 65 dBspl under below conditions:			7	31.7		
System frequency (13 MHz) tolerance ≤ 2.5 ppm			10	25.5		
18 (13 MHz) tolerance ≤ 2.5 ppm 19 32.768KHz tolerance ≤ 30 ppm At least 65 dBspl under below conditions: 1. Ringer set as ringer. 2. Test distance set as 50 cm 2. Test distance set as 50 cm Fast Charge: Typ. 430 mA Slow Charge: Typ. 80mA Total Charging Time: < 3 hours	17	Side Tone Distortion	Three stage distortion < 10%			
(13 MHz) tolerance ≤ 30 ppm At least 65 dBspl under below conditions: 1. Ringer set as ringer. 2. Test distance set as 50 cm Fast Charge: Typ. 430 mA Slow Charge: Typ. 80mA Total Charging Time: < 3 hours	18	System frequency	~ 2.5 nnm			
At least 65 dBspl under below conditions: 1. Ringer set as ringer. 2. Test distance set as 50 cm Fast Charge : Typ. 430 mA Slow Charge : Typ. 80mA Total Charging Time : < 3 hours Bar Number Power 7 -93~ 7→5 -93 ± 2 Antenna Display 5→4 -98 ± 2 4→2 -101 ± 2 2→1 -104 ± 2 1→0 -106 ± 2 0→OFF ~106 Battery Bar Number Voltage 3 ≤3.75 ± 0.05 V		(13 MHz) tolerance	≥ ε.υ μμιι			
20 Ringer Volume 1. Ringer set as ringer. 2. Test distance set as 50 cm Fast Charge : Typ. 430 mA Slow Charge : Typ. 80mA Total Charging Time : < 3 hours	19	32.768KHz tolerance	≤ 30 ppm			
21 Charge Current Fast Charge : Typ. 430 mA Slow Charge : Typ. 80mA Total Charging Time : < 3 hours	20	Ringer Volume	Ringer set as ringer.			
Slow Charge : Typ. 80mA Total Charging Time : < 3 hours Bar Number Power 7 -93~ 7→5 -93 ± 2 4→2 -101 ± 2 2→1 -104 ± 2 1→0 -106 ± 2 0→OFF ~106 Battery Bar Number Voltage 3 ≤ 3.75 ± 0.05 V 23 Battery Indicator			2. Test distance set as 50 cm			
Total Charging Time : < 3 hours Bar Number Power 7 -93~ 7 -93 \pm 2 Antenna Display 5 - 4 -98 \pm 2 4 - 2 -101 \pm 2 2 - 1 -104 \pm 2 1 - 0 -106 \pm 2 0 - OFF ~106 Battery Bar Number Voltage 3 \leq 3.75 \pm 0.05 V	21	Charge Current				
Bar Number Power 7 -93~ 7 $\rightarrow 5$ -93 ± 2 4 $\rightarrow 2$ -101 ± 2 2 $\rightarrow 1$ -104 ± 2 1 $\rightarrow 0$ -106 ± 2 0 \rightarrow OFF ~106 Battery Bar Number Voltage 3 $\leq 3.75 \pm 0.05 \text{ V}$ 23 Battery Indicator $3 \rightarrow 2$	21	Charge Current				
22 Antenna Display						
22 Antenna Display			7	-93~		
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$			7→5	-93 ± 2		
$2 \rightarrow 1 \qquad \qquad -104 \pm 2$ $1 \rightarrow 0 \qquad \qquad -106 \pm 2$ $0 \rightarrow OFF \qquad \sim 106$ Battery Bar Number Voltage $3 \qquad \qquad \leq 3.75 \pm 0.05 V$ 23 Battery Indicator $3 \rightarrow 2 \qquad \qquad 3.75 \pm 0.05 V$	22	Antenna Display	5 → 4	-98 ± 2		
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$			4→2	-101 ±2		
$0 \rightarrow OFF \qquad \sim 106$ $BatteryBarNumber \qquad Voltage$ $3 \qquad \leq 3.75 \pm 0.05V$ $23 BatteryIndicator \qquad 3 \rightarrow 2 \qquad 3.75 \pm 0.05V$			2→1	-104 ± 2		
Battery Bar Number Voltage $ 3 \leq 3.75 \pm 0.05 \text{ V} $ 23 Battery Indicator $ 3 \rightarrow 2 \qquad 3.75 \pm 0.05 \text{ V} $			1 → 0	-106 ± 2		
			0 → OFF	~-106		
23 Battery Indicator 3 → 2 3.75 ± 0.05 V			Battery Bar Number	Voltage		
		Battery Indicator	3	≤ 3.75 ± 0.05 V		
	23		3→2	3.75 ± 0.05 V		
$2 \rightarrow 1$ $3.64 \pm 0.05 \text{ V}$			2→1	3.64 ± 0.05 V		
1 → 0 3.54 ± 0.05 V			1→0	3.54 \pm 0.05 V		

2. SYSTEM SPECIFICATION

Item	Description	Specification
24	Low Voltage Warning	≤ 3.54 ± 0.05V (Call)
24	(Blinking Bar)	≤ 3.4 ± 0.05V (Standby)
25	Forced shut down	3.33 + 0.05V
23	Voltage	3.33 ± 0.03 v
26 Sustain RTCwithout battery Over 50		Over 50 hours
27	Battery Type	Li-lon Battery Standard Voltage = 3.7 V Battery full charge voltage = 4.2 V Capacity: 800mAh
28	Travel Charger	Switching-mode charger Input: 100 ~ 350V, 50/60 Hz Output: 5.1 V, 700 mA

3. TECHNICAL BRIEF

3.1 Digital Main Processor(AD6900, U101)

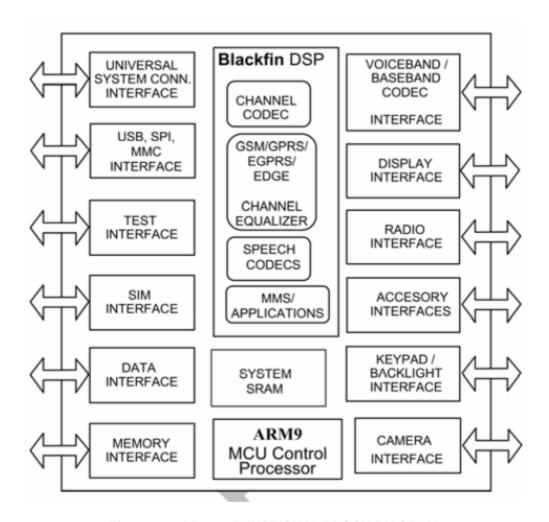


Figure. 3-1 AD6900 FUNCTIONAL BLOCK DIAGRAM

The AD6900 is an advanced, low-power baseband processing solution from Analog Devices, and is part of the AD20msp500 SoftFone® chipset family. The AD6900 is intended for use in a wide variety of feature-rich phones with GSM/GPRS/EGPRS based system connectivity requirements. It is designed to interface easily to an application/OS processor, or to stand alone as a fully integrated and easy-to-use solution for mobile handset and wireless modem applications.

3.1.1 Features of AD6900

Complete Single-Chip Programmable Digital Baseband Processor with four main subsystems

MCU Control Processor Subsystem:

- 32-bit ARM926EJ-S® MCU Control Processor
- 260 MHz operation at 1.5V
- dedicated caches, 16K bytes each, for instructions and data
- 4kB Instruction Tightly Coupled Memory (TCM)
- 2-Mbit On-chip System SRAM
- · Ciphering coprocessor for GPRS supporting GEA1 and GEA2 encryption algorithms
- Kasumi cipher coprocessor for GEA3 encryption
- Dedicated multichannel DMA controller

DSP Subsystem:

- Blackfin 16-bit fixed-point DSP Processor
- 260 MHz operation at 1.5V
- · Memory:
 - → L1 program space: 64 kB SRAM and 16 kB configurable as instruction cache or SRAM
 - → L1 data space: Two banks of 16K bytes, each with 8K bytes of dedicated SRAM and an additional 8K bytes that can be configured as either cache or SRAM
 - → L2 space: 64KB SRAM
- · Ciphering coprocessor (GEA1 and GEA2)
- Kasumi cipher coprocessor for GEA3 encryption
- Dedicated multichannel DMA controller

Peripherals Subsystem:

- Shared on-chip peripherals and off-chip interfaces:
- · Support for Burst-mode, Page-mode, and NAND Flash memory
- Support for SRAM, SDRAM, and PSRAM (cellular RAM)
- Full-Speed USB 2.0 Dual-Role Interface with OTG (On-The-Go) Host Mode or traditional Peripheral-only mode
- · Serial Display Interface
- 8x8 Keypad Interface
- Thumbwheel Interface
- 4 Independent Programmable Backlights plus a Service Light
- 1.8V and 3.0V, 64 kbps SIM Interface
- Universal System Connector Interface
- Multimedia Card (MMC) Interface
- Secure Digital (SD) memory Card Interface and SD I/O
- IrDA transceiver interfaces, including Fast IrDA (4 Mbps baud)
- 2 Configurable Generic Serial Ports (GSPs)
- 7 Configurable Enhanced Generic Serial Ports (eGSPs)

Applications Subsystem for Enhanced Multimedia:

- Parallel Peripheral Interface (PPI) for 10-bit dedicated camera
- sensor or video input interface (including ITU-656 and ITU-601 digital video)
- Separate external bus interface for parallel LCD displays (or camera module inputs)
- reduces noise and loading on the
- · main EBUS interface
- Dedicated multi-channel DMA controller

OTHER FEATURES

- Real-Time Clock (RTC) with Alarm
- Four General-Purpose Timers
- Baseband Converter Interface
- ${\scriptstyle \bullet}$ Compatible with Othello® radio subsystem
- Highly configurable interrupt controller architecture
- Programmable bus arbitration to optimize system performance
- Supports 13 MHz and 26 MHz Input Clocks
- Programmable Power Management and Clock Management
 - Slow Clocking Scheme for Low Idle Mode Current
 - Power Down modes
 - Dynamic Core Voltage Scaling from 1.1 1.5V
- Independent I/O Voltage Domains
- On-chip support for EGPRS Data Services up to Class 10
- Embedded Trace Macrocell for MCU Debug
- JTAG Interface for Test and In-Circuit Emulation of both the MCU and DSP Advanced features for security

DBB ABB Othello™ LEDs Light Controllers CSPORT ADC DAC RAM DAC ADC Filter ADC GMSK DAC 8-PSK DAC Interp MSPORT Filter Filter Headphones ASPORT or Headset Filter DAC Filter Battery Voltage Regulators Charger

3.2 Analog Main Processor(AD6855, U100)

Figure. 3-2-1 AD6855 FUNCTIONAL BLOCK DIAGRAM

The AD6855 is a complete mixed-signal baseband processor that combines all of the data converters and power supply regulators required for a GSM 900 / GSM 850 / DCS 1800 / PCS 1900 mobile on a single device, including HSCSD, GPRS and EGPRS.

3.2.1 General Description

The AD6855 baseband transmit section supports the following mobile station GMSK modulation power classes:

- GSM 900/850 power classes 4 and 5,
- DCS 1800 power classes 1 and 2, and
- PCS 1900 power classes 1 and 2.

The AD6855 baseband transmit section supports the following mobile station 8-PSK modulation power classes:

- GSM 900/850 power classes E2 and E3,
- DCS 1800 power classes E2 and E3, and
- PCS 1900 power classes E2 and E3.

The AD6855 baseband receive section supports GMSK and 8-PSK applications.

The AD6855 auxiliary section provides a voltage reference, an automatic frequency control DAC, an auxiliary ADC, and light controllers. The auxiliary ADC provides two channels for measuring temperature using discrete external devices placed in critical locations. The AD6855 audio section provides 8 kHz and 16 kHz sampling rates for voiceband data input and output and provides nine standard sample rates ranging from 8kHz to 48 kHz for personal audio output on two PCM Audio serial ports. The two Audio serial ports allow support for concurrency. The AD6855 power management section provides voltage regulators for digital and analog components, a battery charger, battery protection circuitry, and power supply activation logic. The AD6855 digital processor interface provides serial ports for control data, baseband transmit and receive data, and two for audio data.

3.2.2 Power Block

CSPORT interface, power management control interface and the circuit that generates power up RESET pulses (RESET2P8 and RESET1P8) for use by the DBB chip.

All regulators except the USB interface regulator are powered from the main battery.

The USB regulator is powered from USB VBUS.

And the user presses KEYON which puts the AD6855 power management system into ACTIVATION state (see definitions below) and signals DBB software that it's time to wake up and operate using the KEYOUT signal.

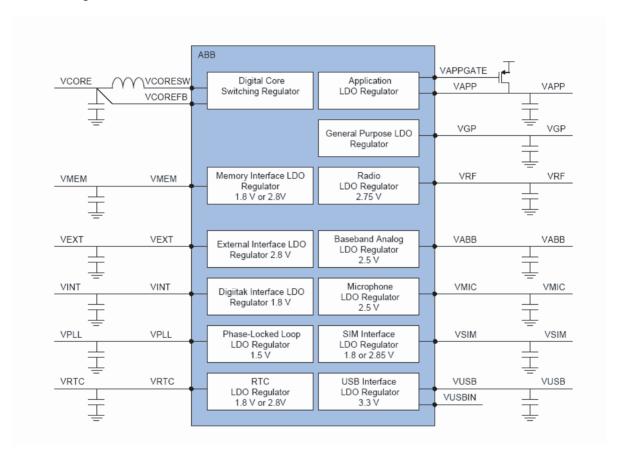


Figure. 3-2-2 AD6855 POWER BLOCK DIAGRAM

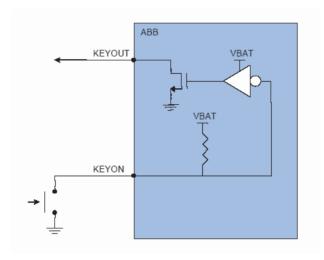


Figure. 3-2-3 AD6855 KEYON/KEYOUT BLOCK DIAGRAM

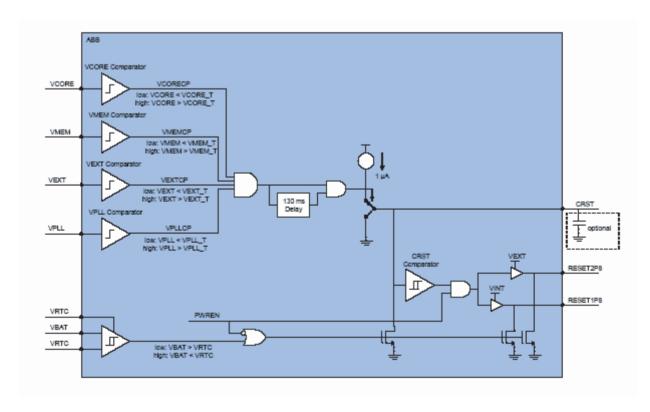


Figure. 3-2-4 AD6855 RESET GENERATION BLOCK DIAGRAM

3. TECHNICAL BRIEF

Power On Reset Generator

The power-on reset signals (RESET1P8 and RESET2P8) are asserted based on the VCORE (if VAPPCFG = 0), VMEM, VEXT, and VPLL regulators. RESET1P8 and RESET2P8 are low when reset is enabled and high when reset is disabled.

When the outputs of all four regulators reach their corresponding threshold voltages, reset will be disabled after a nominal reset period of 130ms.

The outputs of all four regulators must remain at or above their corresponding threshold voltages for the duration of the reset period for reset to be disabled (pulled high).

The nominal 130ms reset period is restarted whenever all four regulators reach their threshold voltages. The nominal reset period of 130ms can be extended by connecting an external capacitor to CRST. This capacitor is charged using a small current when reset is enabled. Once the capacitor reaches the threshold, reset is disabled.

Reset will be enabled immediately if any one of the four regulators falls below their corresponding threshold voltages. In addition, reset will be enabled if VBAT falls below VRTC. The PWREN signal is the logical AND of all the state controls that enable or disable many of the regulators on the chip. If the regulators enabled by PWREN are disabled by PMT state controls described below then PWREN must go low.

When PWREN goes low reset will be immediately enabled causing RESET1P8 and RESET2P8 to be pulled low.

When reset is enabled, both RESET1P8 and RESET2P8 are actively pulled low. CRST is also actively pulled low when reset is enabled.

VABB Regulator Enable/Disable Logic Operation

The VABB regulator powers many on-chip analog circuits on the ABB. The VCXOEN signal, the VABBEn bit in the LDOControl1 Bit Positions (Addr 0x35) register, and the AFCDACMode and AFCDACOn bits in the AuxControl1 Bit Positions (Addr 0x13) register all participate in controlling the VABB enable/disable.

When the ABB power management system transitions from Off state, DDLO state, UVLO state, or Thermal Shutdown State to Power Key Activation, Charger Activation, USB Charger Activation, or Active State VABB will be enabled. During these state transitions ABBEn = 0 and AFCDACMode = 0, VRF is enabled.

Once the ABB power management system is in Power Key Activation, Charger Activation, USB Charger Activation, Active-Standby or Active State the VABB regulator enable/disable is controlled by the information written to the VABBEn and AFCDACMode register bits by system software.

Digital Baseband Core (VCORE)

The Digital Baseband Core regulator supplies the digital baseband processor (DBB) core.

The voltage on VCORE is selectable using the VCOREControl register.

The VCOREActive code selects the voltage on VCORE in high power mode and the VCOREStandby code selects the voltage on VCORE in low-power mode.

DBB Interface (VINT)

The DBB interface regulator supplies the DBB/ABB digital interfaces. The output voltage of the VINT regulator is nominal 1.8V.

Memory (VMEM)

The VMEM regulator supplies the external memory(s) and the interface to the external memory on the digital baseband processor. The output voltage of the Memory Interface regulator can be selected as 1.8V nominal or 2.8V nominal using the VMEMSEL terminal.

External Interface (VEXT)

The External Interface regulator supplies the Radio digital interface and the high voltage (>1.8V) interface between the digital baseband processor and various peripherals, such as the LED indicators and the LCD display.

SIM Interface (VSIM)

AD6855 is designed to support 3.0 V and 1.8 V SIMs exclusively (i.e. no 5 V SIMs).

The SIM Interface regulator supplies the SIM interface circuitry on the digital processor and the SIM card. By default the SIM Interface regulator output is 2.85 V, which can be decreased to 1.8 V if a 1.8 V SIM is detected.

Real-Time Clock (VRTC)

The Real-Time Clock regulator supplies the Real-Time Clock module. The Real-Time Clock regulator is optimized for low ground current.

Baseband Analog (VABB)

The Baseband Analog regulator supplies the analog portions of the AD6855. Operation of the VABB regulator is controlled by the VABBEn bit in the LDOControl1 register.

If VABBEn = 0, the VABB regultor will be disabled unless the AFCDAC is enabled or VCXOEN = 1. If VABBEn = 1 (the default state) VABB is enabled along with VCORE, VMEM, and VEXT. The Baseband Analog regulator is optimized for high ripple rejection and low noise. The output of the Baseband Analog regulator should not be used as a supply for any external components.

3. TECHNICAL BRIEF

Microphone (VMIC)

The Microphone regulator supplies the microphone interface circuitry. The Microphone regulator is optimized for extremely high ripple rejection up to 217 Hz and low noise.

VRF (VRF)

The VCXO regulator supplies the voltage controlled crystal oscillator (VCXO). The VCXO regulator is optimized for high ripple rejection and low noise.

USB Interface (VUSB)

The VUSB regulator supplies the USB transceiver located in the DBB. Digital Baseband PLL (VPLL) The VPLL regulator supplies the phase locked loop on the digital baseband (DBB).

General Purpose Regulator (VGP)

The General Purpose regulator is intended primarily to serve as a supply rail for camera modules. Its voltage is programmable by setting VGPSel[3:0] in theLDOControl2 Register. VGP is enabled by setting the VGPEn bit in LDOControl1 to 1.

Applications Regulator (VAPP)

The VAPP regulator is an adjustable regulator that uses an off chip pass device. It has two modes of operation selected by the state of the VAPPCFG terminal. If VAPPCFG is pulled low the VAPP regulator functions as a programmable voltage applications supply.

In this mode, VAPP is enabled or disabled using the VAPPEn bit of LDOControl1.

3.3 Power Amplifier Module(SKY77318, U601)

3.3.1 Internal Block Diagram

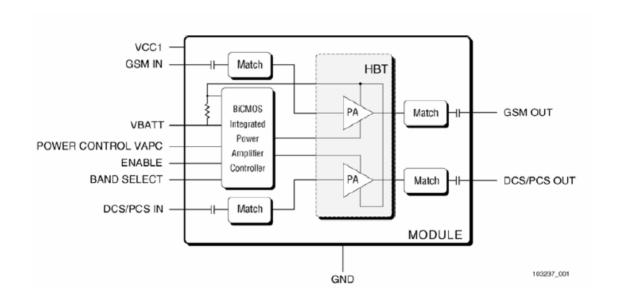


Figure. 3-3-1 SKY77318 FUNCTIONAL BLOCK DIAGRAM

3.3.2 General Description

The SKY77318 Power Amplifier Module (PAM) is designed in a low profile (1.2 mm), compact form factor for quad-band cellular handsets comprising GSM850/900, DCS1800, and PCS1900 operation. The PAM also supports Class 12 General Packet Radio Service (GPRS) multi-slot operation. The module consists of separate GSM PA and DCS1800/PCS1900 PA blocks, impedance-matching circuitry for 50 ߟ input and output impedances and a Power Amplifier Control (PAC) block with an internal current-sense resistor. The custom BiCMOS integrated circuit provides the internal PAC function and interface circuitry.

Fabricated onto a single Gallium Arsenide (GaAs) die, one Hetero-junction Bipolar Transistor (HBT) PA block supports the GSM bands and the other supports the DCS1800 and PCS1900 bands. Both PA blocks share common power supply pins to distribute current.

3.4 FEM (DGM1110M014, FL601)

	ANT_SW1	ANT_SW2
GSM850/900 TX	L	Н
DCS/PCS TX	Н	Н
GSM850/900 RX	L	L
DCS/PCS RX	Н	L

Figure 3-4-1 Band SW Logic Table

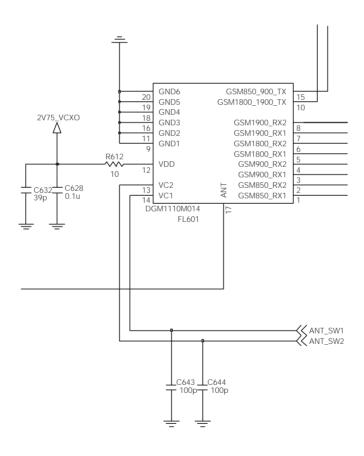


Figure 3-4-2 FEM CIRCUIT DIAGRAM

The FEM is integrated of quadband RX SAWs, internal diplexer and ESD protection at Ant port to 8kV acc.

3.5 RTC(FC-135, X100)

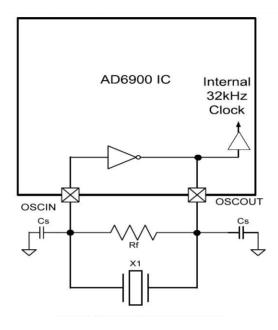


Figure. 3-5-1 32.768KHz Crystal Basic Connections

The AD6900 supports a Real Time Clock function. A total of 25pF+/-10% capacitance to graound is required (including board trace capacitance) on each OSCIN and OSCOUT.

RTC functionality allows the application software to implement standard clock, calendar, or organizer functions.

A 32KHz clock is required in AD6900 based systems to take advantage of power saving "slow clocking" mode. A combination of an oscillator circuit within the AD6900 IC and an external 32KHz crystal results in a stable 32kHz clock for use in the system. The purpose of this application note is to discuss the system issues that affect operation of the 32kHz oscillator circuit.

3.6 Crystal(26 MHz, X601)

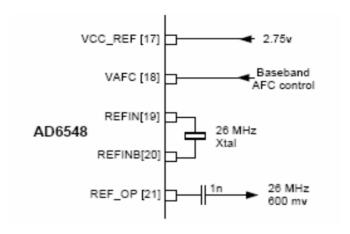


Figure. 3-6-1 Crystal Oscillator External Connection

The AD6548 requires only an external low cost as the frequency reference. The circuitry to oscillate the crystal and tune its frequency is fully integrated. The Oscillator is a balanced implementation requiring the crystal to be connected across 2 pins. There is a programmable capacitor array included for coarse tuning of fixed offsets, and an integrated varactor for dynamic control. The oscillator is designed for use with a 26MHz crystal. The crystal is connected as shown in figure 3-3.

Dedicated control software ensures excellent frequency stability under all circumstances. The AD6548 reference oscillators provides a 26MHz 600mVpp (typical) output (REF_OP), for use as the baseband clock input.

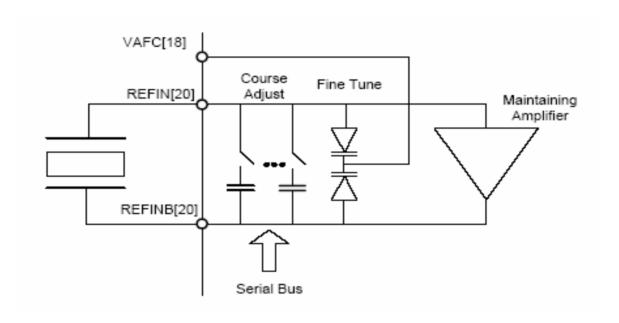


Figure. 3-6-2 Crystal Circuit Block Diagram

The AD6548 integrates this frequency tuning range the tuning section comprises a switchable capacitor array for discrete steps and varactor for fine tuning. Contol of the tuning process is driven by software, whereby the frequency can be maintained accurately during reception gaps and initial frequency upon startup can be accurately estimated without the need for temperature sensors.

VCC TXVCO AD6548 PA Module ΤX TXOP LO RX Antenna Switch Module RX85 VCC BB RX850 TXC RX90 DC Offset TXQE RX900 Correction RX1800 DC Offset RX1800 RXQ RX1900 RX1900 RXQE AFC) RXLO Xtal Osc Frac-N Synth + Tuning TX LO Generator CLK SDATA Serial SCLK LDO LDO VCC REF REF OF Interface Rea 2 Rea 1 SEN Rea 3 VLD01 VLD03

3.7 RF Tranceiver(AD6548, U602)

Figure. 3-7-1 CIRCUIT DIAGRAM of RF Tranceiver

3.7.1 GENERAL DESCRIPTION

The AD6548 provides a highly integrated direct conversion radio solution that combines, on a single chip, all radio and power management functions necessary to build the most compact GSM radio solution possible. The only external components required for a complete radio design are the Rx SAWs, PA, Switchplexer and a few passives enabling an extremely small cost effective GSM Radio solution.

The AD6548 uses the industry proven direct conversion receiver architecture of the OthelloTM family. For Quad band applications the front end features four fully integrated programmable gain differential LNAs. The RF is then downconverted by quadrature mixers and then fed to the baseband programmable-gain amplifiers and active filters for channel selection. The Receiver output pins can be directly connected to the baseband analog processor. The Receive path features automatic calibration and tracking to remove DC offsets.

The transmitter features a translation-loop architecture for directly modulating baseband signals onto the integrated TX VCO. The translation-loop modulator and TX VCO are extremely low noise removing the need for external SAW filters prior to the PA.

The AD6548 uses a single integrated LO VCO for both the receive and the transmit circuits. The synthesizer lock times are optimized for GPRS applications up to and including class 12.

3.7.2 FUNCTIONAL DESCRIPTION

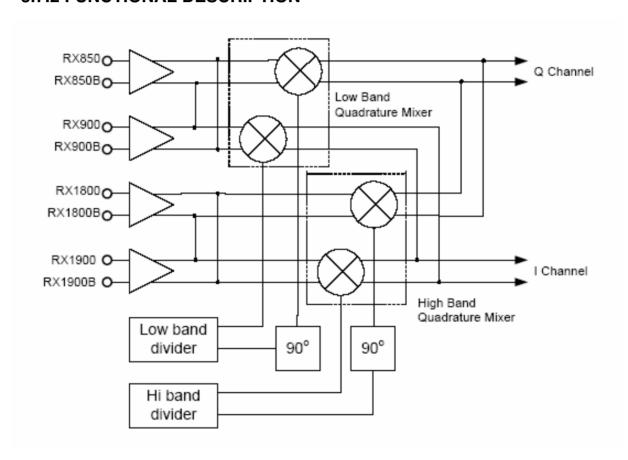


Figure. 3-7-2 RECEIVER CHAIN BLOCK DIAGRAM

3. TECHNICAL BRIEF

3.7.2.1 RECEIVER CHAIN

The AD6548/9 receiver section fully integrates all the RF and baseband signal processing. Each major block is described in the following sections.

Low Noise Amplifiers

The AD6548 includes four fully integrated Low Noise Amplifiers (LNAs), to support quad band applications without further external active components. The LNAs have differential inputs which minimize the effect of unwanted interferers. The inputs are easily matched to industry standard Front End Modules (FEMs) or discrete Rx SAW filters. The outputs of the LNAs are directly coupled to the down-converting mixers.

The voltage gain of the LNAs are typically 24 dB. Each LNA can be switch to a low gain mode when receiving large input signals as part of the AGC system.

Down-Converting Mixers Two quadrature mixers are used to mix down the signals from the LNAs, one for the high bands (1800 and 1900 MHz) and one for the low bands (850 and 900 MHz). The outputs of the mixers are connected to the baseband section through an integrated single pole filter with nominal cut-off frequency of 800kHz. This acts as a "roofing filter" for the largest blocking signals (i.e. those ≥ 3MHz) and prevents the baseband amplifiers from being overloaded.

Baseband Amplifiers / Low Pass Filters

The baseband amplifiers provide the majority of the analog receiver gain. The filtering is provided by an integrated 5th order Chebyshev filter giving the necessary adjacent channel and blocking filtering, it is also acting as an anti-alias filtering for Baseband IC's converters. A final low pass pole is possible Baseband Output D.C. Offset Correction In order to minimize D.C. offsets inherent in the receiver and maximize dynamic range a D.C offset correction circuit is integrated. This correction is triggered over the serial bus and then an offset tracking loop is enabled to minimize residual offsets under all conditions. The tracking loop is fully hardware integrated, requiring no software intervention.

Receiver Local Oscillator (LO) Generator

The Rx LO generator is used to avoid DC offset problems associated with LO leakage into the receiver RF path. By operating the VCO at a frequency other than the desired receive frequencies, any leakage of the VCO will fall out of band. The LO generator is used to convert the offset synthesized VCO output to the on-frequency quadrature LO required by the chipset. The LO generator is implemented as a regenerative frequency divider, performing a 2/3 multiplication of the VCO output for the high band (DCS1800/PCS1900) and a 1/3 multiplication for low band (E-GSM 900/GSM850).

3.7.2.2 Transmit Path

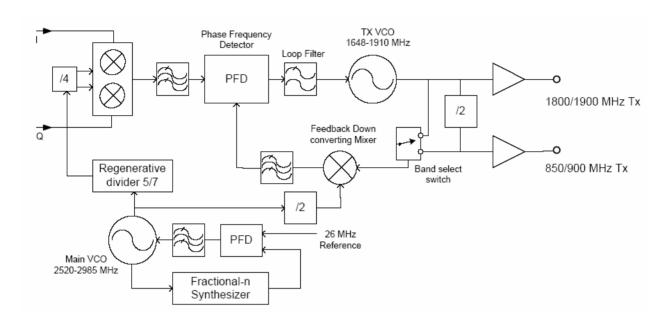


Figure. 3-7-3 TRANSMIT PATH BLOCK DIAGRAM

Overview

The transmit section of the AD6548/9 radio implements a translation loop modulator.

This consists of a quadrature modulator, high speed phase-frequency detector (PFD) with charge pump output, loop filter, TX VCO and a feedback down converting mixer. The VCO output (divided by 2 for low band) is fed to the power amplifier with a portion internally fed back into the down-converting feedback mixer to close the feedback loop.

Quadrature Modulator

The Quadrature modulator takes the baseband I & Q signals and translates these into a GMSK signal at the Transmit Intermediate Frequency (TX IF). After bandpass filtering and limiting the TX IF signal is used as the reference input to the Phase Frequency Detector (PFD) of the transmit PLL.

3. TECHNICAL BRIEF

Phase Frequency Detector (PFD)

The PFD ensures that the transmitted signal contains the required modulation and is accurately locked to the desired GSM channel. The downconverted feedback signal from the TX VCO and the Quadrature Modulator output are phase compared by the PFD.

The PFD charge pump generates a current pulse proportional to the difference in phase which is applied to the loop filter.

Loop filter

To minimize complexity of the external PCB layout the TX loop filter is fully integrated into the IC. At power up the filter is automatically calibrated as part of the baseband filter cal, eliminating process tolerances. The calibration is fully integrated and requires no extra programming.

TX VCO

The Transmit Voltage Controlled Oscillator (TX VCO) and tank components are a fully integrated subsystem. The subsystem includes PA drivers so the outputs are used to directly drive the external PAs. The low noise oscillator design and internal filtering mean that external TX SAW filters are not required. In Low band operation the TX VCO output is divided by two and filtered. The TX VCO is automatically calibrated to ensure optimum performance over its operating frequency of 1648 to 1910 MHz.

Feedback Down-Converting Mixer

The feedback down converting mixer is used to translate the TX VCO output frequency to the TX IF. An integrated band pass filter exists between the mixer and the PFD to filter the mixers unwanted side band and higher order mixing products.

3.7.2.3 Main Frequency Synthesizer

The AD6548 has a single fast-locking fractional synthesizer used for VCO control in both receive and transmit mode. The entire system including VCO, tank, fractional N dividers, sigma delta compensation, charge pump and loop filters are fully integrated.

The only external component is the frequency reference. The synthesizer is controlled via the serial interface. The VCO is fed into the respective dividers to generate the appropriate LO frequencies for the RX and TX bands.

Fractional N Dividers

The fractional N divider allows the PLL system to have a smaller step size than theb comparison frequency which is set by the external reference to 26 MHz. This feature allows all the GSM frequency band rasters to be achieved, with fast lock times and good phase noise characteristics. The divider section consists of a dual modulus 8/9 prescaler, integer M & A dividers, and fractional N system based on sigma-delta modulation to generate the required fractional divide ratio. The Denominator of the fractional divider can be set to 3 different values, (1040, 1170, 1235), depending on the mode of operation. For example a denominator of 1040 with an input fraction F maintains an average value of F/1040 allowing 25 kHz steps when operated at a reference of 26 MHz. The Overall count value is thus:

8*M + A + Fraction

Where: M is 4 bits, but the MSB is set to 1. A is 3 Bits, Fraction is N/ Denominator.

The Denominator is set to one of 3 values: 1040, 1170, 1235. N is a 11 bit value.

Values for M, A and N are loaded from serial interface word, but the denominator is automatically set according to the mode.

Refer to the Programming Procedures for more details.

Phase Frequency Detector/Charge Pump

A Phase Frequency Detector (PFD) is used for the PLL phase detector. The charge pump is designed such that good matching of up and down currents is achieved over a wide output operating range. The charge pump output is internally routed to the integrated synthesizer loop filter.

Synthesizer Loop filter

To minimize complexity of the external PCB layout the Main Synthesizer loop filter is also fully integrated into the IC. No external components or adjustments are required.

Voltage Controlled Oscillator

The integrated voltage controlled oscillator (VCO) is a complete self-calibrating subsystem. This employs a fully automated digital self-calibration function to ensure optimum phase noise performance over the entire frequency range. The VCO generates frequencies between 2520MHz and 2985MHz as required to operate in the four GSM bands for RX and TX.

Sibley with LPSDRAM Device Family Flash Die Options F1-CE# -F2-CE# F-WP1# -Flash Die #2 Flash Die #1 (512 or 256 Mbit) (512 or 256 Mbit) F-RST# F-CLK -F-ADV# -F-VCC F-WP2# -F-WAIT ◀ F-VPP OE# WE# -Flash Die #3 Flash Die #4 (512 or 256 Mbit) (512 or 256 Mbit) F3-CE# -F4-CE# VCCQ DQ[15:0] -VSS A[MAX:MIN] LPSDRAM Die Options D-VCC D-DM[1:0] -LPSDRAM Die #1 D-WE# -(512 or 256 or 128 Mbit) D1-CS# D-BA[1:0] -D-CAS# D2-CS# LPSDRAM Die#2 D-RAS# -(512 or 256 or 128 Mbit) D-CLK -D-CKE -

3.8 MEMORY(PF38F5060M0Y0BE, U202)

Figure. 3-8-1 MEMORY BLOCK DIAGRAM

The 512Mbit Ballaire Wireless Flash memory with LPSDRAM stacked device family offers multiple high-performance solutions. The Ballaire flash die is manufactured on 65 n m ETOX™IX Process Technology. It delivers 108 MHz synchronous burst and pagemode read rates with supports multipartitioning with Read-While-Write (RWW) or Read-While-Erase (RWE) dual operations. The LPSDRAM is a high-performance volatile memory operating at speeds up to 133 MHz with configurable burst lengths.

The Ballaire stacked device features programmable driver strength and low-power operation.

This Stacked Chip Scale Package (SCSP) device is packaged in a standard Intel® x16D footprint and signal ballout.

This model uses 512Mbits Flash memory and 128Mbits LPSDRAM memory with stacked.

The DBB External Bus Interface provides a memory-mapped interface to external devices such as NOR Flash, NAND Flash, SRAM, SDRAM, PSRAM, and other custom devices.

The External Memory Interface contains three distinct memory controllers: a NAND Flash Controller (NFC), an SDRAM Controller (SDC), and the External Bus Controller (EBC).

These three controllers share the external pins. They also share an arbiter through which the DMA controllers (via DDBUS, ADBUS, and DMABUS) and the processor cores (via DSPBUS and MCUEBUS) access external devices. The following figure shows the external memory interface block diagram.

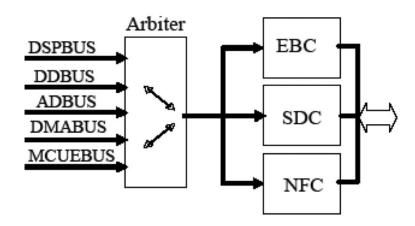


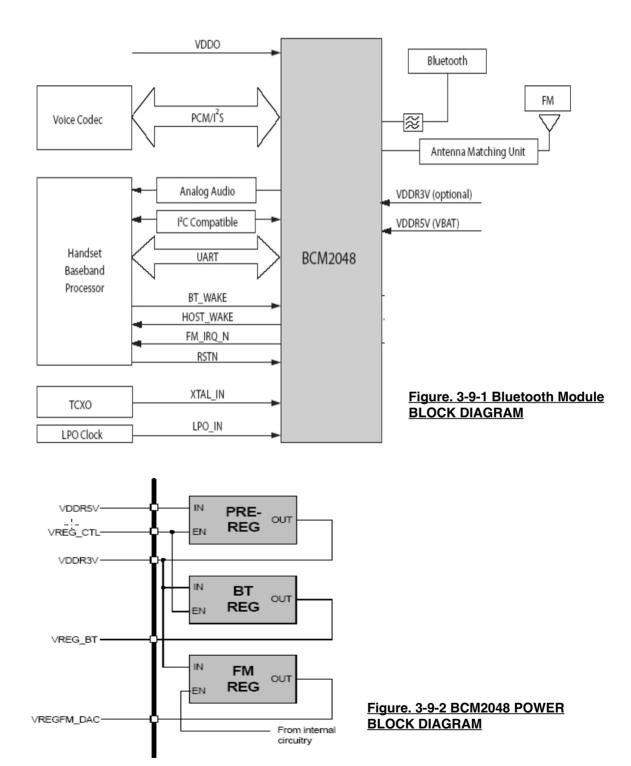
Figure. 3-8-2 DBB EBU SUBSYSTEM BLOCK DIAGRAM

The following table shows the pin list for the external memory interface which supported by Main Base Band chipset(AD6900).

3. TECHNICAL BRIEF

Signal Name	Function
DATA[15:0]	Data
ADDR[25:0]	Address
nWE	Write Enable
nRD	Read Enable
nADV	Valid Address
nA0CS	General Purpose Chip Select
nA1CS	General Purpose Chip Select
nA2CS	General Purpose Chip Select
nA3CS	General Purpose Chip Select
nA4CS	General Purpose Chip Select
nA5CS	General Purpose Chip Select
nSDCS	SDRAM Chip Select
nNDCS	NAND Flash Chip Select
nB0CS	Auxiliary Chip Select
nB1CS	Auxiliary Chip Select
nHWR / nUBS/ SDQM[1] / CLE	High Write / Byte Strobe / Data Mask/ Command Latch Enable
nLWR / nLBS / SDQM[0] / ALE	Low Write / Byte Strobe / Data Mask / Address Latch Enable
BURSTCLK	Burst Memory Clock
nWAIT	External Device Wait Input
nSDRAS	SDC Row Address Strobe
nSDCAS	SDC Column Address Strobe
nSDWE	SDC Write Enable
SDA10	SDC address 10
SDCKE	SDC Clock Enable
SDCLKOUT	SDC Clock Output
nNDBUSY	NFC Busy Request

3.9 BT Module with integrated FM tuner (EWFMLBAXX, U201)



3. TECHNICAL BRIEF

3.9.1 Power Block

To reduce the external BOM, the BCM2048 features three internal voltage regulators for the Bluetooth and FM sections that eliminate the need for filtering between the digital and noise sensitive RF circuits. These regulators operate from either 2.3V to 5.5V input supplies that support direct connection to Lithium batteries, or to a 1.7V to 3.6V input supply.

The pre-regulator, PRE-REG, regulates battery power supply down to a level acceptable to the internal main regulators, BT REG and FM REG. The PRE-REG and the BT REG are enabled by an external input VREG_CTL. If VREG_CTL is low, the BCM2048 is shut down. If preregulation is not required because the input power supply is in the range 1.7V to 3.6V, VDDR5V and VDDR3V should be tied together to form the input power supply.

For more on supplying power to the BCM2048, refer to the reference schematic document, available from your Broadcom representative.

3.9.2 Operational Description

The BCM2048 Bluetooth radio transceiver provides enhanced radio performance to meet the most stringent industrial temperature applications and the tightest integration into mobile handsets and portable devices. It is fully compatible with all standard TCXO frequencies and provides full radio compatibility to operate simultaneously with GPS and cellular radios. It also integrates a complete FM and RDS/RBDS solution. The integrated solution saves power and board space, minimizes the BOM, and maximizes interface flexibility over a separate Bluetooth and FM solution. The FM subsystem can operate independently of Bluetooth and achieve full performance while Bluetooth is operating. It is designed to cover from 76 MHz, up to 108 MHz, bands (US, Europe, Japan) and to operate from either the Bluetooth reference clock or a 32-kHz LPO input. The FM subsystem supports a conventional I2C compatible interface and analog outputs for legacy systems, as well as digital interface options, such as I2S and PCM. The I2S and PCM interfaces supports 48-kHz operation and can be either master or slave. The analog interface consists of high-quality, line-level stereo DACs. The BCM2048 FM subsystem includes advanced RDS/RBDS capability. The BCM2048 synchronizes, demodulates, and decodes RDS/RBDS signals including CRC processing, post data filter detection, signal quality estimation, and buffering thus making it easy for an external application to read and process the RDS/RBDS data. The FM radio provides excellent reception, with 1 •ÏV for 26 dB (S+N)/N typical sensitivity and greater than 60-dB SNDR capability, allowing easier system integration and antenna design. The FM subsystem includes many sought-after features, including signal-dependant mono/stereo blend, soft mute, and signal bandwidth control. The system has digital RSSI, signal quality, and IF frequency error indicators for system monitoring. The FM subsystem contains embedded automatic search and scan features, and large RDS data buffers to simplify the interface with an external host.

3.10 SIM Card Interface

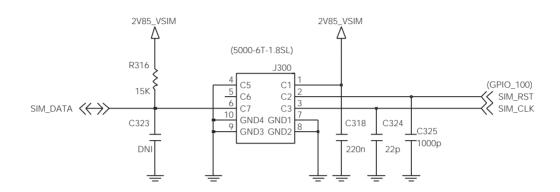


Figure 3-10. SIM CARD Interface

The Main Base Band Processor(AD6900) provides SIM Interface Module.

The AD6900 checks status Periodically During established call mode whether SIM card is inserted or not, but it doesn't check during deep sleep mode. In order to communicate with SIM card, 3 signals SIM_DATA, SIM_CLK, SIM_RST.

And This model supports only 3V SIM Card.

Signals	Description	
SIM_RST	This signal makes SIM card to HW default status.	
SIM_CLK	This signal is transferred to SIM card.	
SIM_DATA	This signal is interface datum.	

3.11 Micro-SD Card Interface

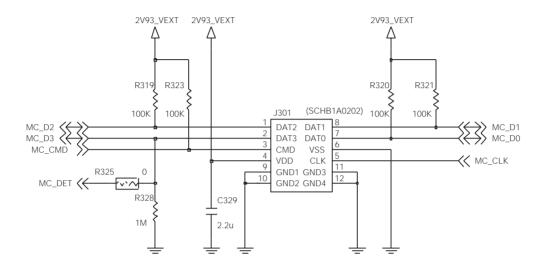


Figure 3-11. Micro-SD Interface

AD6900 provides an interface for Multi-Media Cards (MMC), Secure Digital Memory Cards (SD Card), and Secure Digital Input/Output Cards (SDIO). All of these cards use similar interface protocols. The main difference between MMC and SD support is the initialization sequence. The main difference between SD card and SDIO support is the use of interrupt and read wait signals for SDIO.

Features of the MMC/SD interface (MMCI) include:

- · Support for a single MMC, SD Memory or SDIO card
- Support for 1-bit and 4-bit SD modes (SPI mode is not supported)
- A six-pin external interface with clock, command, and up to 4 data lines
- Card detection using one of the data pins
- Card interface clock generation from SYSCLK
- SDIO interrupt and read wait features

The following table lists the six pins in the MMCI

The MMCI consists of an MMC/SD controller along with a peripheral bus interface.

The controller handles the multi-media and secure digital card functions. This includes clock generation, power management, command transfer, and data transfer. The bus interface contains 32-bit memory mapped registers, converts 16-bit PBUS accesses to 32-bit register accesses,

3.12 LCD Interface

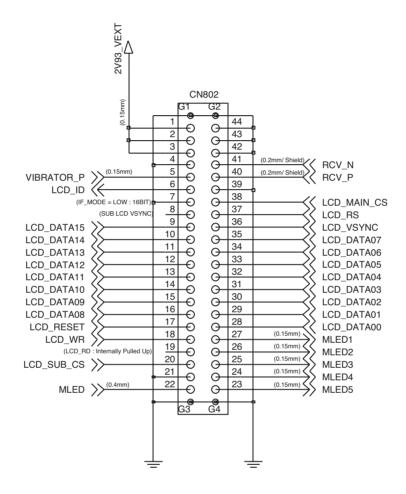


Figure 3-12-1. LCD Interface

LCD Module provides 2 LCD, Primary LCD(240x320, 262K Color) and Secondary LCD(128x160, 262k Color).

The controller handles the multi-media and secure digital card functions. This includes clock generation, power management, command transfer, and data transfer. The bus interface contains 32-bit memory mapped registers, converts 16-bit PBUS accesses to 32-bit register accesses,

Two LCD shared Data bus, RD, WR and RS but CS (chip select signal).

BLU (Back Light Unit) is shared primary and secondary LCD and include 5 white LEDs. White LCD driver is AAT3169 and it is descripted at next page.

LCD BACKLIGHT

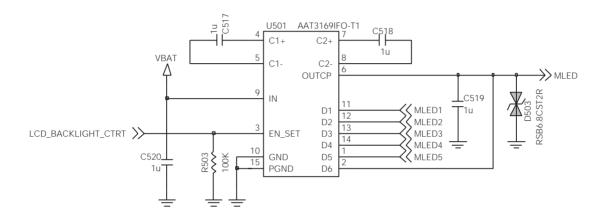


Figure 3-12-2. AAT3169 CIRCUIT DIAGRAM

The AAT3169 is a low noise, constant frequency charge pump DC/DC converter that uses a tri-mode load switch (1X), fractional (1.5X), and doubling (2X) conversion to maximize efficiency for white LED applications. The AAT3169 is capable of driving six LEDs for a total of 180mA from a 2.7V to 5.5V input. The current sinks may be operated individually or in parallel for driving higher current LEDs.

A low external parts count (two 1μ F flying capacitors and two small 1μ F capacitors at IN and OUTCP) make this part ideally suited for small, battery-powered applications.

AnalogicTech's AS2CwireTM (Advanced Simple Serial ControlTM) serial digital input is used to enable, disable, and set current for each LED with a 16-level logarithmic scale plus four low-current settings down to 115μ A. For optimized efficiency, low-current settings require only 65μ A of housekeeping current.

Each output of the AAT3169 is equipped with builtin protection for output short-circuit and auto-disable for load short-circuit conditions. Built-in softstart circuitry prevents excessive inrush current during start-up. A low-current shutdown feature disconnects the load from the input and reduces quiescent current to less than 1μ A.

The AAT3169 can setup three group as Maximum current, 15mA, 20mA and 30mA Each group has 16 steps of 2 stages as current level, so totally has 32 steps.

One stage is about high current and the other stage is about low current.

Refer to Detail feature below.

Data	Mean 30mA Max	Mean 20mA Max	Mean 15mA Max
1	30.0	20.0	15.0
2	29.3	19.5	14.6
3	27.8	18.5	13.9
4	25.2	17.5	12.7
5	22.8	15.4	11.5
6	20.9	14.2	10.5
7	18.5	12.5	9.3
8	16.1	10.9	8.1
9	13.7	9.3	7.0
10	10.0	8.0	6.0
11	9.4	6.5	4.9
12	7.0	4.9	3.7
13	4.7	3.3	2.6
14	3.3	2.4	1.9
15	1.9	1.5	1.2
16	0.0	0.0	0.0

Data	Main Low Current On	Sub Low Current On	Current
1	No	No	
2	No	No	
3	No	No	
4	No	No	
5	No	Yes	115µA
6	No	Yes	175µA
7	No	Yes	280µA
8	No	Yes	400µA
9	Yes	No	115µA
10	Yes	No	175µA
11	Yes	No	280µA
12	Yes	No	400µA
13	Yes	Yes	115µA
14	Yes	Yes	175µA
15	Yes	Yes	280µA
16	Yes	Yes	400µA

Figure 3-12-3 AAT3169 High Current Stage

Figure 3-12-4 AAT3169 Low Current Stage

This model uses level 5 in maximum 20mA group and level 15 in low current mode. But it don't use low current stage.

3.13 Battery Charger Interface

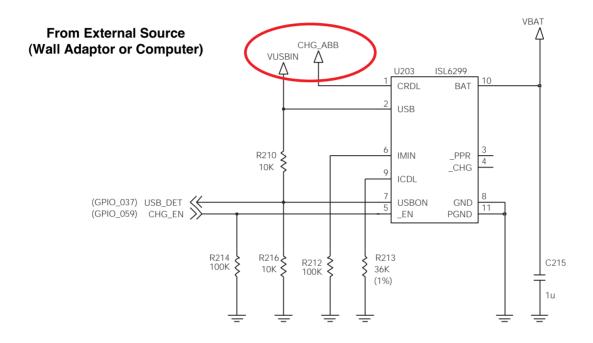


Figure 3-13 BATTERY CHARGER BLOCK

The ISL6299 is a fully integrated low-cost single-cell Li-ion or Li-polymer battery charger. The charger accepts two power inputs, normally one from a USB port and the Other from a desktop cradle. The ISL6299 is an ideal charger for smart handheld devices that need to communicate with a personal computer via USB.

The ISL6299 features 28V and 7V maximum voltages for the cradle and the USB inputs respectively. Due to the 28V rating for the cradle input, low-cost, large output tolerance adapters can be used safely. When both inputs are powered, the cradle input is used to charge the battery.

3.14 Keypad Interface

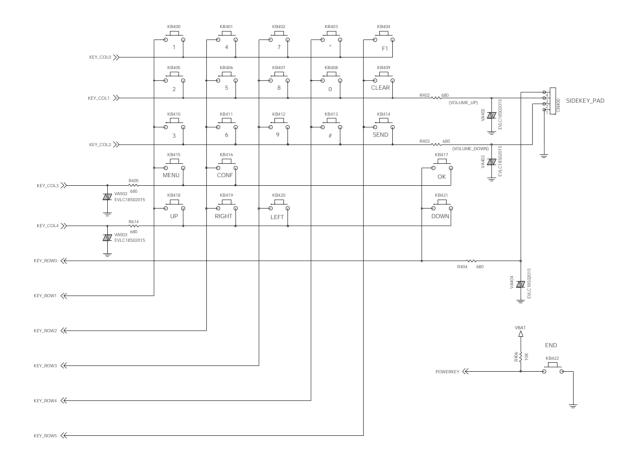


Figure 3-14-1 MAIN KEY STRUCTURE

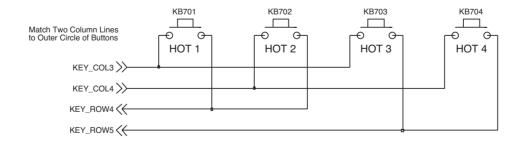


Figure 3-14-2 HOT KEY STRUCTURE

The keypad interface supports a row/column decoding of a keyboard matrix of up to 8 rows and 8 columns. The interface generates an interrupt when any key is pressed, and the interrupt is routed through the system interrupt controller to the MCU. Software must scan the columns to determine which key was pressed. Debouncing must also be implemented in software. The keypad interface consists of eight tristateable KEYPADCOL outputs and eight KEYPADROW inputs. Pressing a key pulls the corresponding KEYPADROW input low. When all KEYPADCOL outputs are driven low, pulling any KEYPADROW input low generates an interrupt.

In the interrupt service routine, the keypad must be scanned by setting only one column output low at a time and reading the row inputs. A zero is read anywhere a key is pressed on that column. The scan should be repeated at regular intervals until no key is being pressed. To implement debouncing, the software must require the same scan result for several scans. The keypad interrupt should not be cleared until no key has been pressed for several scans.

The 8 by 8 matrix of rows and columns provides the possibility of up to 64 keys (with an additional 8 if a ghost column is used). Full flexibility in enabling and disabling individual rows and columns is provided. Any rows or columns not used should be disabled in the Keypad Control Register. The following figure shows the keypad interface and interrupt generation logic.

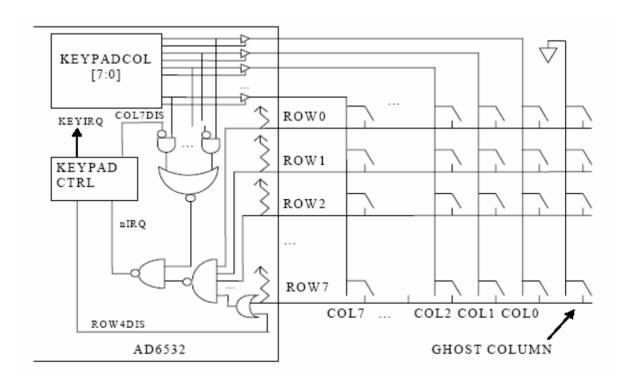


Figure 3-14-3 keypad interface and interrupt generation logic

ABB DBB Filter Music MSES Serial Port MSDI (MSPORT) Filter Analog Filter + Switch ASFS Headphones ASDI Audio Filter Serial Port (ASPORT) ASDO Microphone

3.15 Audio Interface

Figure 3-15-1 ABB Internal Audio Block Diagram

The AD6855 Audio Section supports communications and personal audio applications.

The Audio Section provides an audio codec with two digital-to-analog converters and an analog-to-digital converter, a microphone interface, and analog input and output channels.

Audio and Music Serial Ports

The AD6855 Audio Serial Port is described in detail in the Audio Serial Port (ASPORT) section below. AD6855 Music serial port (MSPORT) is described in detail in the Music Serial Port (MSPORT) section below.

Audio Codec

The AD6855 audio codec supports communications applications with digital sample rates of 8 kHz or 16kHz. DAC 1 is used for receiving speech. An ADC is used for sending speech. The AD6855 audio codec supports personal audio applications with digital sample rates of 8 kHz, 11.025kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, or 48 kHz. DAC 1 and DAC 2 are used for monophonic audio. The channels are common in the digital section. DAC 1 and DAC 2 are used together for stereo audio, with DAC 1 decoding the left-channel digital input and DAC 2 decoding the right-channel digital input.

3. TECHNICAL BRIEF

Audio codec operating modes can be controlled by writing 5 bit codes in the AudMode field of the AudControl1 register and in the AudMode_M field of the AudControl4 register.

AudControl1 programs the sampling rate and stereo or monophonic operating mode for PCM audio samples input via the ASPORT.

AudControl4 programs the sampling rate and stereo or monophonic operating mode for PCM audio samples input via the MSPORT.

The AudControl1 and AudControl4 contain control bits that allow system software to turn on three audio loudness enhancement techniques meant for use when driving 8 ohm loudspeakers. These are high pass filter, dynamic range compressor, and x4 gain boost.

These loudness enhancement techniques can be used with any AudMode or AudMode_M setting. And are programmed seperately and independently for the ASPORT and MSPORT PCM audio decoder data streams.

Analog Audio Output & Input Configurations

Output configurations are set by AudOS[4:0] bits in the AudControl2 register. Input configurations are set by AudIS[3:0] bits in the AudControl2 register.

AudIn3LMute bit high in the AudMuteControl register (0x27). For configurations using "DAC2+AIN3R", the AIN3R input may be muted by setting AudIn3RMute bit high in the AudMuteControl register. For configurations using "AIN3(L)", the AIN3L and AIN3R inputs may be used as a differential input or the AIN3L input may be used as a single-ended input.

Single ended configuration is chosen by setting AudIn3Cfg bit high in the AudControl3 register (0x32).

Audio DACs and Analog Filters

The Audio DACs are over-sampled switched-capacitor DACs. The analog filters are switched-capacitor filters followed by active-RC filters.

Analog Audio Output Drivers

Audio Output 1

PGA gain for Audio Output 1 can be set by using bits AudOut1Gain[4:0] in the AudOut12Control (0x21) register. Output 1 is used for 32ߟ interface with differential output but can be used by single ended interface.

And this model only uses passive filters between output port and Receiver.

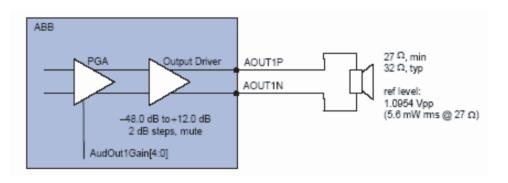


Figure 3-15-2 ABB Audio OUTPUT1

Audio Output 2

PGA gain for Audio Output 2 can be set by using bits AudOut2Gain[4:0] in the AudOut12Control (0x21) register. Output 2 is used for 8ߟ. This port supports only a differential interface. And this model only uses passive filters and Class D audio amplifier between output port and speaker. Audio amplifier Gain is set by hardware component and gain is 6 times.

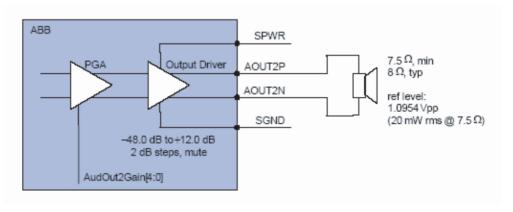


Figure 3-15-3 ABB Audio OUTPUT2

Audio Output 3

PGA gain for Audio Output 3 Stereo Configuration can be set by using bits AudOutLGain[4:0] and AudOutRGain[4:0] in the AudOutLRControl (0x22) register. When Audio Output 3 configured as monophonic differential output PGA gain can be set by using bits AudOut3Gain[4:0] in the AudOut3Control register (0x23).

This port is used for headset speaker in stereo. This port must use DC-coupling capacitor as output DC. It uses two 100uF capacitor each other in left and right output.

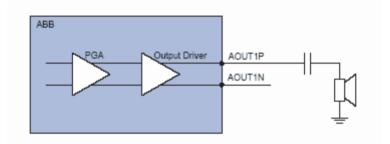


Figure 3-15-3 ABB Audio OUTPUT3

Analog Audio Input

The AD6855 provides two analog input channels, AIN1 and AIN2, that may be used for both microphone and line inputs. The AIN1 and AIN2 channels are identical. One of the two channels is typically used with microphone built into a handset. The other channel is typically used with an external microphone or external line input.

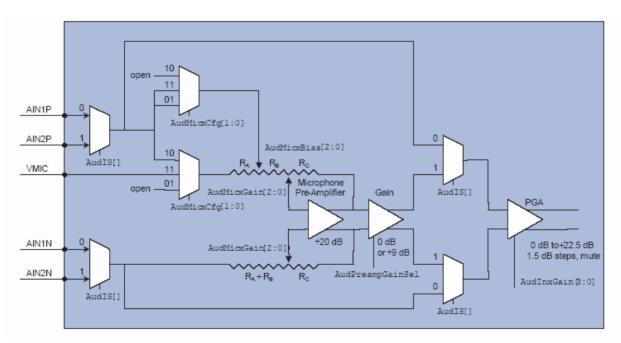


Figure 3-15-4 Audio Input Block Diagram

Analog Input AIN1, AIN2 and VMIC configurations can be chosen by setting bits AudIS[3:0] in the AudControl2 register (0x1E). Additional gain of 9dB can be inserted into Analog Audio Input signal chain by setting AudPreampGainSel bit high in the AudControl3 register (0x32).

Microphone Interface

The microphone pre-amplifier and associated integrated resistors support electret microphones. An internal (Configuration 11) or external (Configuration 01 or 10) load resistor converts the current input of the microphone to a voltage signal which is amplified using a low-noise pre-amplifier. The Microphone signal path also includes an additional programmable gain of +9 dB gain directly after the pre-amplifier. Different microphones require different DC bias currents for optimum sensitivity.

Audio ADC and PGA

The Audio ADC is a high-order single-bit sigma-delta ADC that includes a switchedcapacitor PGA at the input.

Digital Filters

The AD6855 Audio Section provides two digital filters. The voiceband filter is used for applications with a 8 kHz digital sample rate. The high-quality audio filter is used for applications with higher digital sample rates.

Audio Accessory Detection

The AD6855 provides for detection of audio headset accessory insertion, extraction, and hookswitch events. The detector circuit is designed to operate with minimum power in standby mode. There are two pins dedicated to the accessory detector. AccDet is intended to interface to the external microphone and monitor its bias voltage. The ACCDET terminal is used to sense hookswitch events while a headset accessory is inserted. The JackSense terminal is interfaced to the switch pin of the Jack socket or a Jack Sense terminal on a handset system connector.

3. TECHNICAL BRIEF

Use of the AccDet Terminal for Hookswitch Event Detection

The AccDet terminal may be connected directly to the Ain2P pin in the case of a DC coupling of the accessory microphone. If the accessory microphone is connected via a capacitor then the AccDet pin may be connected to the microphone side of the coupling capacitor. The AccDet terminal is used to detect hookswitch events. Hookswitch events cause the system to answer an incoming phone call or hang up on an active phone call.

The detector circuit is in operation only if an accessory is inserted. It monitors the voltage at the AccDet terminal using a comparator as shown Figure below.

Associated logic then provides the AudAccInt interrupt and updates the contents of the Detector Control register as follows on each comparator transition.

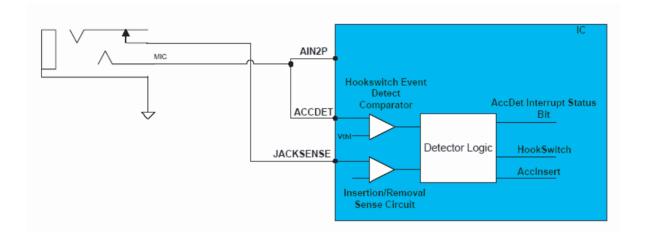


Figure 3-15-5 Audio Accessory Detection Block Diagram

Use of the JackSense Terminal for Accessory Insertion and Removal Detection

Accessory insertion and removal is detected using the JackSense terminal.

The JackSense terminal is connected to a signal produced by a mechanical connection that indicates the presence or absence of the headset accessory. The insertion/removal sense circuit fed by JackSense is flexible as far as the characteristics of the mechanical connection are concerned. The mechanical connection will often times be pulled down in one state and floating in the other. In such cases a 1uA on chip current source is used to pull JsckSense to VBAT when the mechanical connection is floating.

To avoid false interrupts the Accessory detect logic has a hardware polling loop which will prevent Interrupt generation from comparator transitions with a duration of no less than 10 mSec.

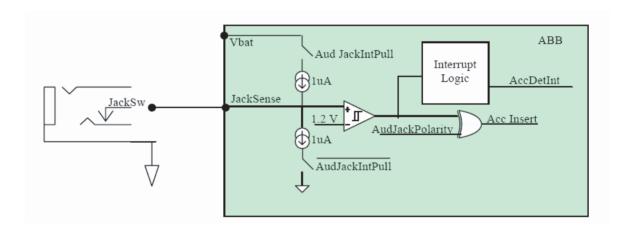


Figure 3-15-6 Accessory Insertion/Removal Detector Block Diagram

3.16 Camera Interface(2M Fixed Focus Camera)

3.16.1 AD6900 Camera Interface (PPI Block)

AD6900 provides a Parallel Peripheral Interface (PPI) that can connect directly to camera modules. The PPI is an input-only parallel external port that accommodates up to 10 bits of data, in a variety of RGB and YUV color formats. In addition, ITU-656 (CCIR656) and ITU-601 (CCIR601) compatible data transfers are supported.

The PPI feature set includes:

- Eight dedicated data pins and two data pins muxed with GPIOs
- Parallel data transfer rates up to 32.5 MB/s
- Two frame syncs (horizontal and vertical), with programmable polarity
- A bidirectional clock pin, with programmable output clock rate up to 65 MHz
- · Synchronization by detection of embedded preamble codes or by using frame synchronization pins
- ITU standard and counter controlled data transfers
- 8-bit data packing to reduce DMA bandwidth for image data
- Data re-ordering to reduce DMA bandwidth for YUV 4:2:2 data
- A 32 word by 16 bit input FIFO

The PPI offers specific configurations to support still image and video data inputs.

The PPI supports ITU-601 and ITU-656 standards. It also provides Active Video Only and Entire Field operational modes. In all modes, data packing options optimize DMA transfer bandwidth for YUV 4:2:2 and other data formats.

The PPI pins are listed in the following table.

Signal Name	Function	Default	Direction
PPI_DATA[7]	Data		Input
PPI_DATA[6]	Data		Input
PPI_DATA[5]	Data		Input
PPI_DATA[4]	Data		Input
PPI_DATA[3]	Data		Input
PPI_DATA[2]	Data		Input
PPI_DATA[1]	Data		Input
PPI_DATA[0]	Data		Input
PPI_DATA_10B_LSB[1]	Optional Data		Input
PPI_DATA_10B_LSB[0]	Optional Data		Input
PPI_HSYNC	Frame Sync		Input
PPI_VSYNC	Frame Sync		Input
PPI_CLK	Clock	Input	Bi-Directional

PPI Architecture

A simplified PPI block diagram is shown in the following figure. The PPI contains a 32 word by 16 bit FIFO, interrupt request (IRQ) generation logic, clock dividers, and memory mapped registers(MMRs). The PPI provides a parallel interface to camera modules.

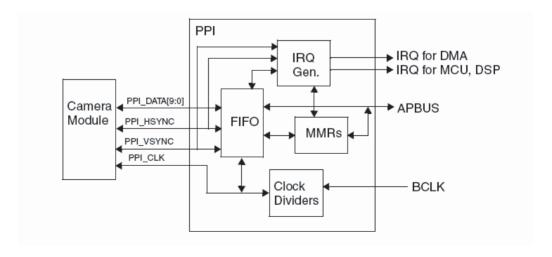


Figure 3-16-1 PPI Block Diagram

3. TECHNICAL BRIEF

FIFO Operation

The PPI FIFO is 32 words by 16 bits. Received data is stored in the FIFO either as 16- bit words or as 8-bit words. The data is only stored a 8-bit words when the DLEN and PACK_EN bits in the PPI Control register are cleared. The data in the FIFO may be read whenever the FIFO is not empty. The DMA controllers may burst read the FIFO data whenever at least four words are contained in the FIFO. These FIFO status conditions are reported in the PPI Status register and can be unmasked in the PPI DMA Interrupt Mask register to generate interrupts.

Interrupt Request Generation

The PPI generates interrupt requests for the DMA controllers, MCU, and DSP.

An interrupt can be generated for the following conditions:

- Start of a frame
- FIFO overflow
- FIFO underflow
- Incorrect number of data words in a line or lines in a frame
- Preamble code error (in ITU-656 mode)

PPI Clock Frequency

The PPI transfer clock may be provided either by an external source or internally by the PPI. BCLK is the source for the PPI clock divider. The clock may be divided by 1, 2, 3, 4, 5, 6, 7,8, 16, 32 or 64 from BCLK. However, the maximum frequency supported is 32.5 MHz for packed 8-bit transfers and 16.25 MHz for 10-bit or unpacked 8-bit transfers. At higher clock frequencies, the APPDMA does not support the incoming data bandwidth. A PPI FIFO (32 words deep, 16-bits wide) is provided to compensate for arbitration latency encountered by APP DMA accessing system resources.

3.17 KEY BACLKLIGHT LED Interface

The AD6855 Auxiliary Section provides three independent PWM light controllers. The PWM output controllers regulate the average current through active lights.

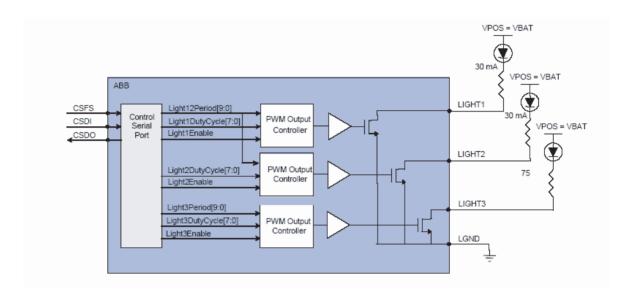


Figure 3-17 ABB Light Controller Block Diagram

The output frequencies of the LIGHTx PWM output controllers are set by the Light12Period (0x2F) and Light3Period (0x31) control registers.

With fMCLK = 13 MHz, frequencies ranging from 50.781 kHz to 49.591 Hz may be specified.

```
fLIGHT1 = (fMCLK / 256) / (Light12Period[9:0] + 1)
fLIGHT2 = (fMCLK / 256) / (Light12Period[9:0] + 1)
fLIGHT3 = (fMCLK / 256) / (Light3Period[9:0] + 1)
```

he output duty cycles of the PWM output controllers are set by the LightxDutyCycle[7:0] control registers - Light1DutyCycle (0x2D), Light2DutyCycle (0x2E) and Light3DutyCycle (0x30).

This model use only Light3 port and 2 high luminance white LED with light guard film.

3.18 Vibrator Interface

Vibrator is drived by Dual BJT with bias resistor.

VIBRATOR_P is connected with + terminal of vibrator and - terminal is connected with Ground. It is controlled by VIBRATOR signal of DBB with only ON/OFF function.

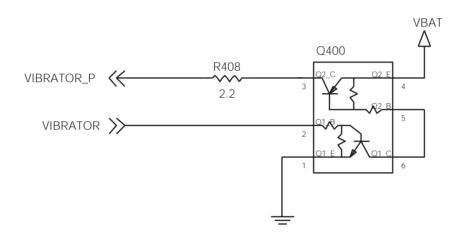


Figure 3-18 Vibrator Driver Block Diagram

4. TROUBLE SHOOTING

4.1 RF Component

TEST POINT

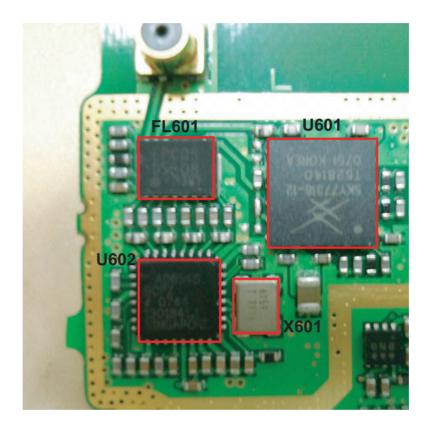
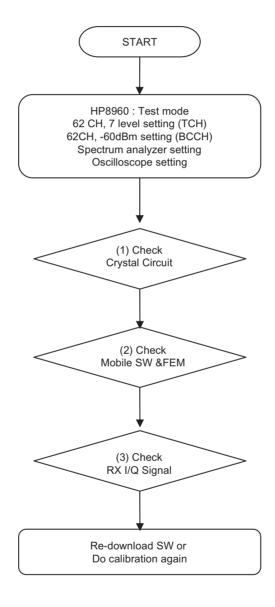


Figure 4-1

U601	Power Amp Module (SKY77318)	
U602 (AD6548)	RF Main Chip (Transceiver)	
X601	Crystal, 26MHz Clock	
FL601	FEM	

4.2 RX Trouble



(1) Checking Crystal Circuit

TEST POINT

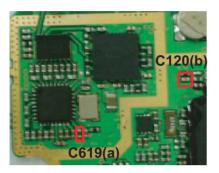
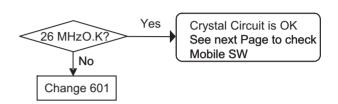
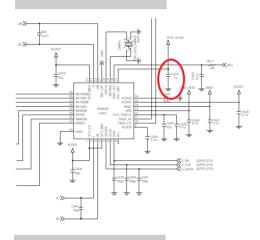


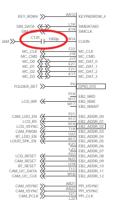
Figure 4-2-1

CHECKING FLOW

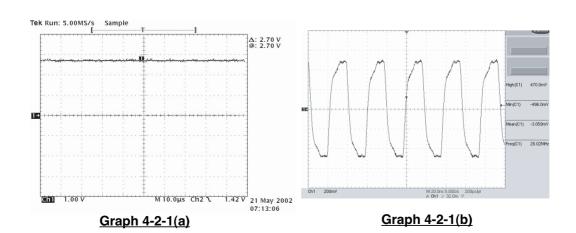


CIRCUIT





WAVEFORM



(2) Checking Mobile SW & FEM

TEST POINT

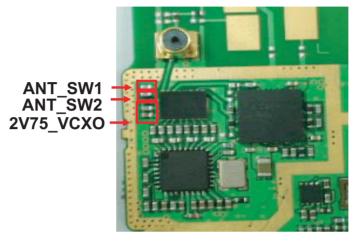
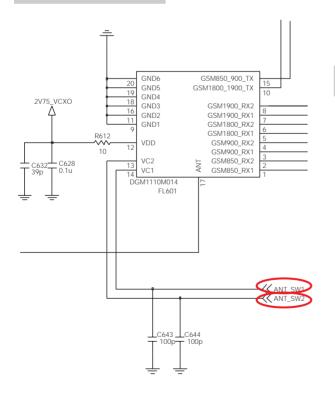


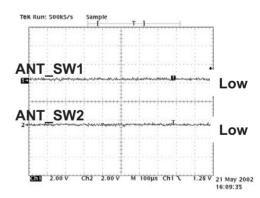
Figure 4-2-2

CIRCUIT

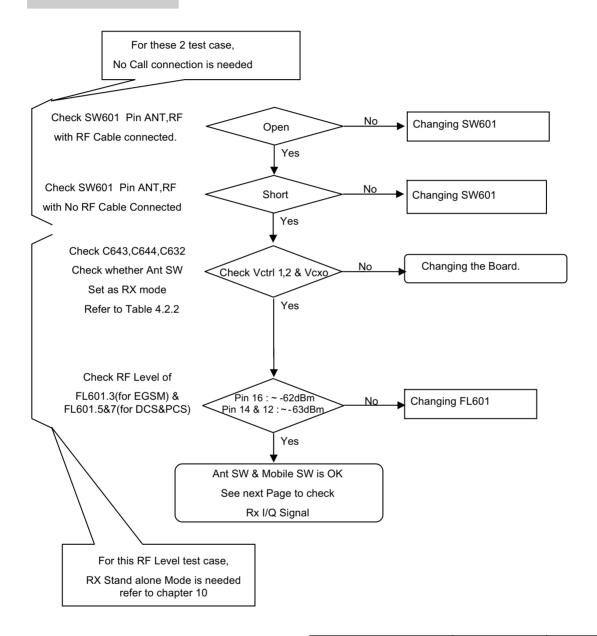


WAVEFORM

EGSM RX



Graph 4-2-2 FEM Control Signal



Switch Mode	Vc1	Vc2
GSM850/900 Tx	0	1
GSM1800/1900 Tx	1	1
GSM850/900 Rx	0	0
GSM1800/1900 Rx	1	0

Table 4.2.1

4. TROUBLE SHOOTING

(3) Checking RX I/Q

TEST POINT

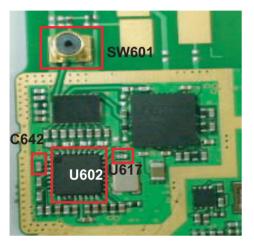
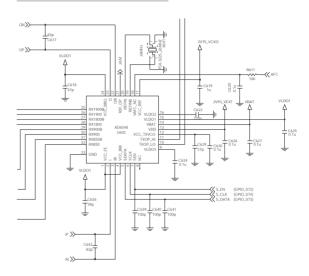
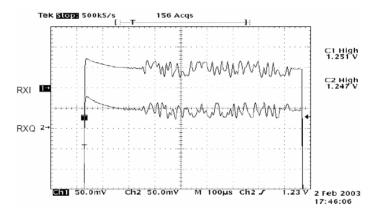


Figure 4-2-3

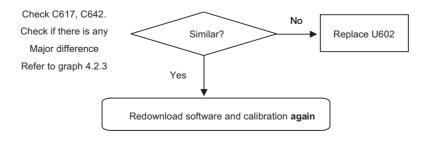
CIRCUIT



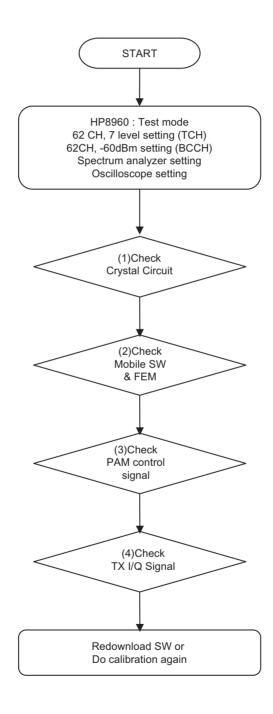
WAVEFORM



Graph 4-2-3



4.3 TX Trouble



(1) Checking Crystal Circuit

TEST POINT

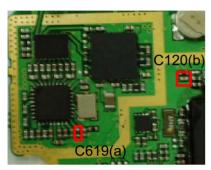
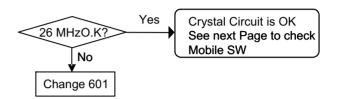
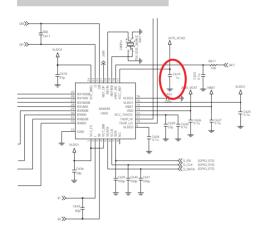


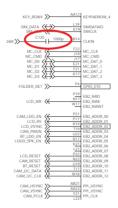
Figure 4-3-1

CHECKING FLOW

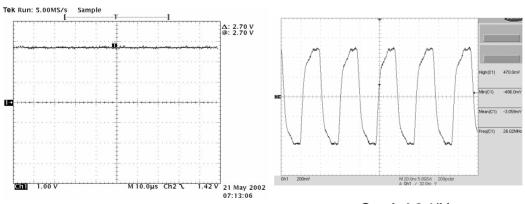


CIRCUIT





WAVEFORM



<u>Graph 4-3-1(a)</u> <u>Graph 4-3-1(b)</u>

(2) Checking Mobile SW & FEM

TEST POINT

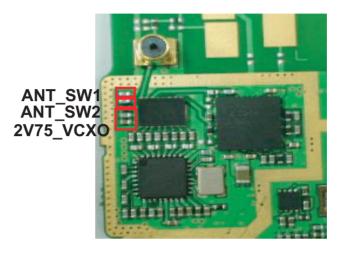
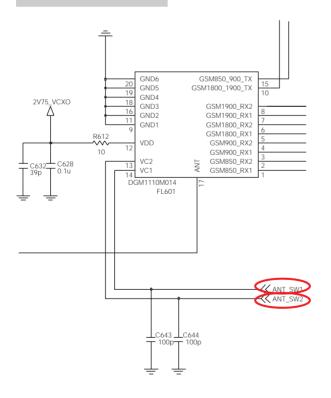


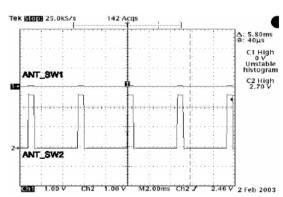
Figure 4-3-2

CIRCUIT

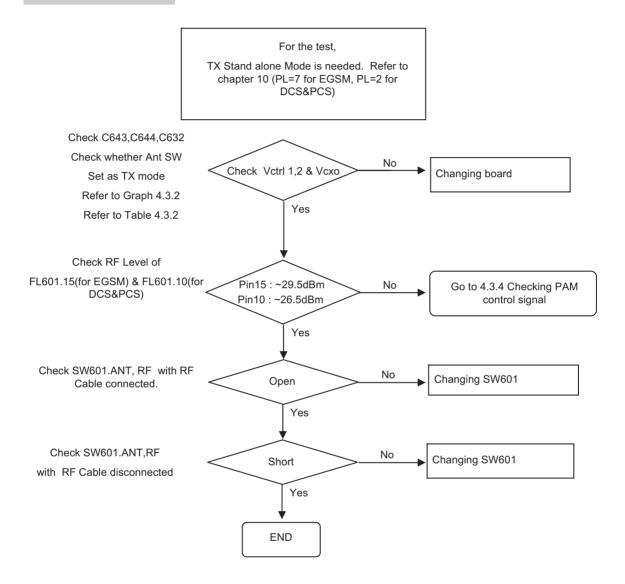


WAVEFORM

EGSM Tx



Graph 4-3-2 FEM Control Signal



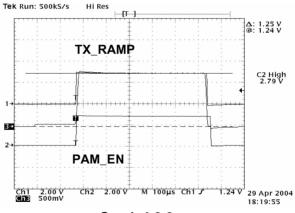
Switch Mode	Vc1	Vc2
GSM850/900 Tx	0	1
GSM1800/1900 Tx	1	1
GSM850/900 Rx	0	0
GSM1800/1900 Rx	1	0

Table 4-3-1

(3) Checking PAM Control Signal

TEST POINT CIRCUIT VBAT COSS_COSS_COSS_COSS_D SET_ORGE COSS_COSS_COSS_D SET_ORGE COSS_COSS_D SET_ORGE COSS_COSS_COSS_D SET_ORGE COSS_COSS_D SET

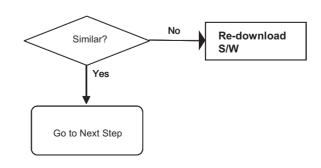
WAVEFORM



Graph 4-3-3

CHECKING FLOW

Check TX_RAMP and PAM_EN
Check if there is
Any Major Difference or not
Refer to Graph 4.3.3



4. TROUBLE SHOOTING

(4) Checking TX I/Q

TEST POINT

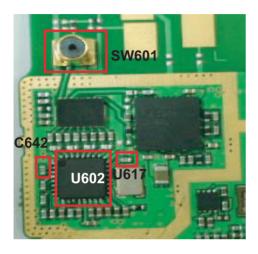
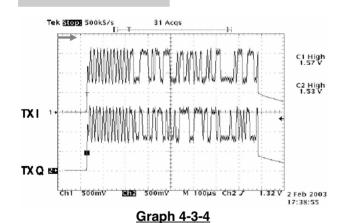


Figure 4-3-4

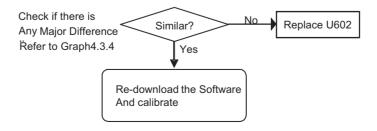
CN) VLDO1 VLDD1 VLDD1 VLDD1 VLDD1 VLDD1 VLDD1 VLDD1 VLDD

CIRCUIT

WAVEFORM

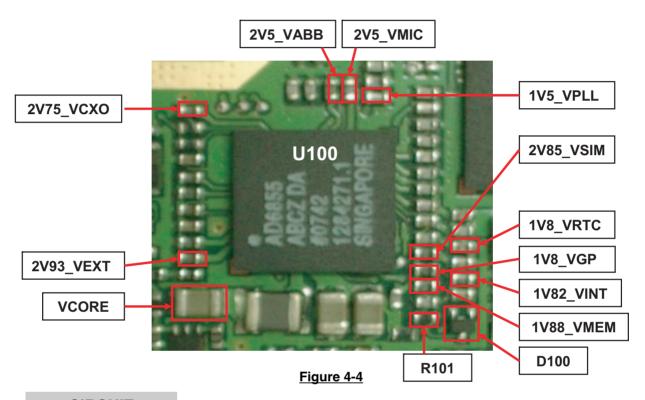


CHECKING FLOW

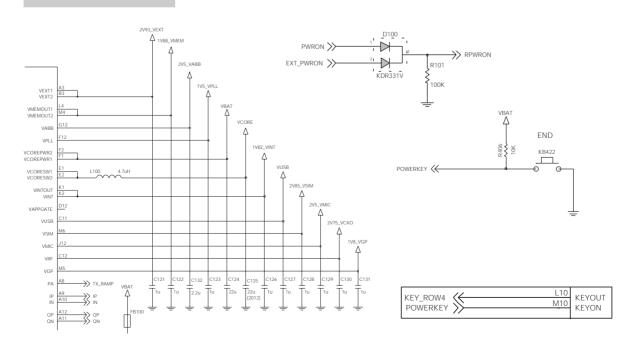


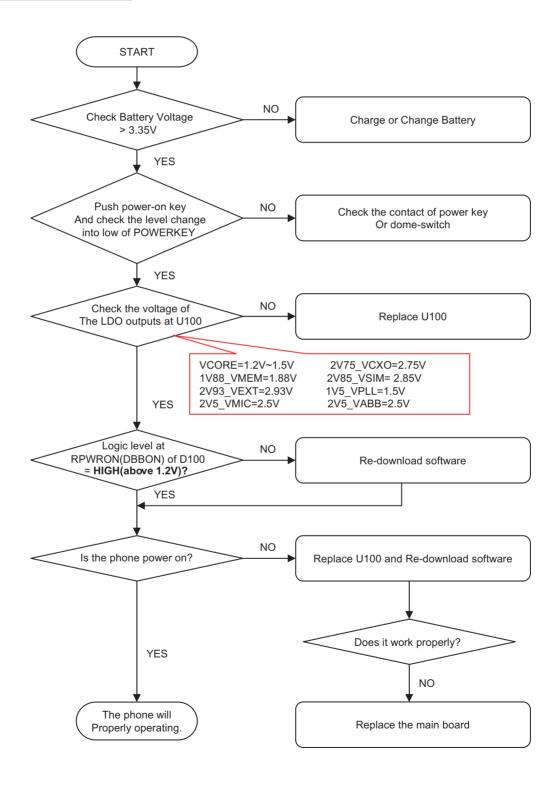
4.4 Power On Trouble

TEST POINT



CIRCUIT





4.5 Charging Trouble

TEST POINT

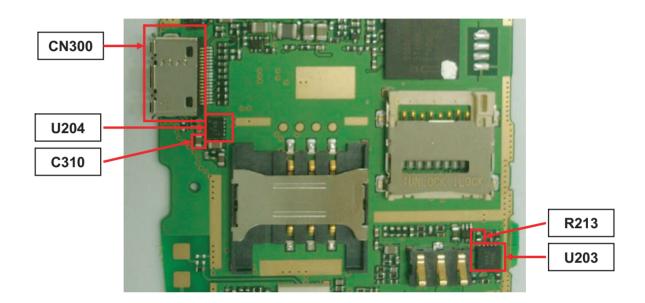
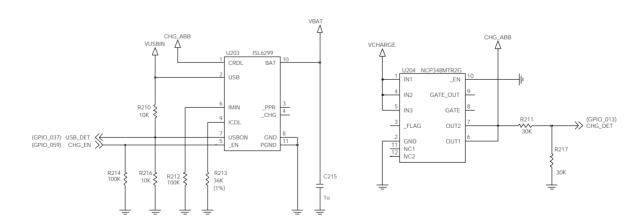
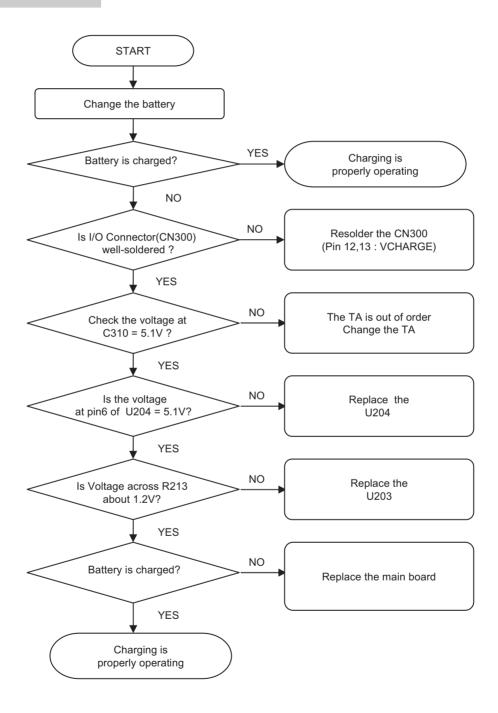


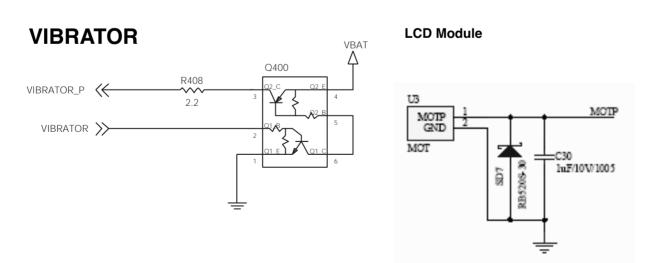
Figure 4-5



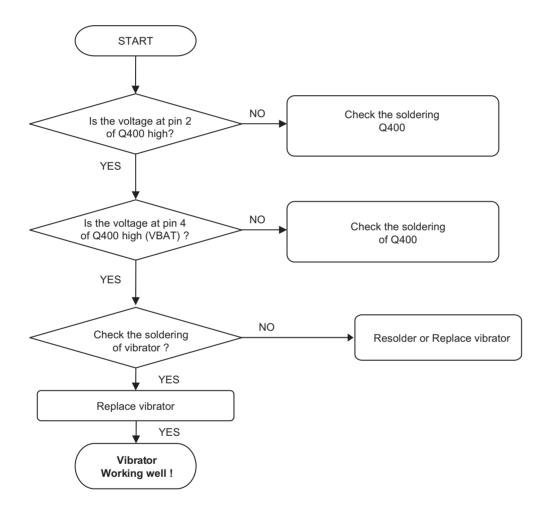


4.6 Vibrator Trouble

TEST POINT PIN 1 Q400 Vibrator PAD Figure 4-6

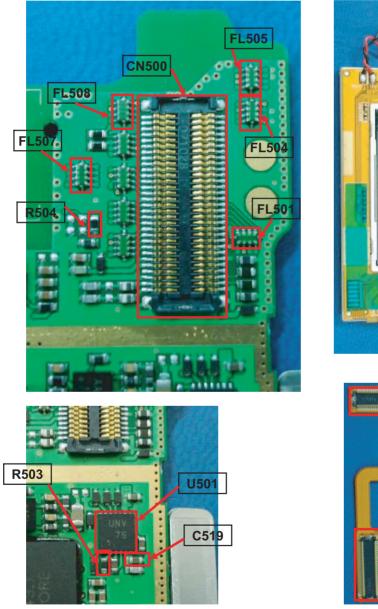


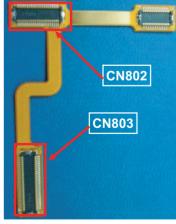
SETTING: Enter the engineering mode, and set vibrator on at vibration of BB test menu



4.7 LCD Trouble

TEST POINT



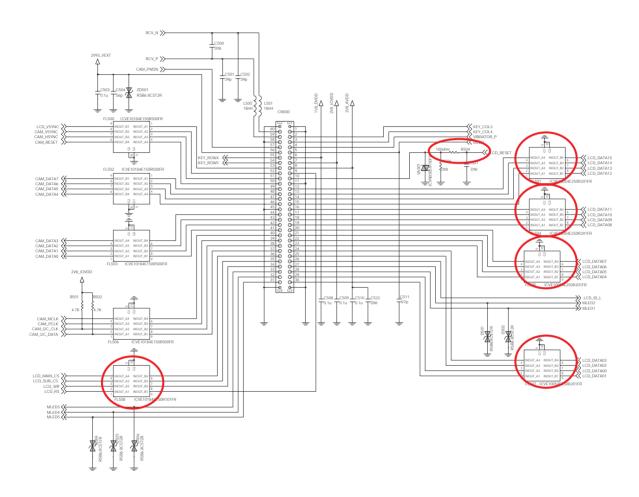


LCD Connector

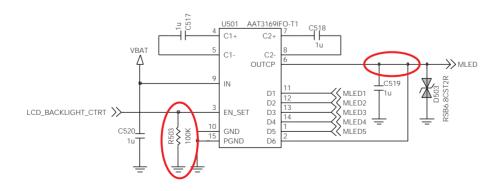
Figure 4-7

CIRCUIT

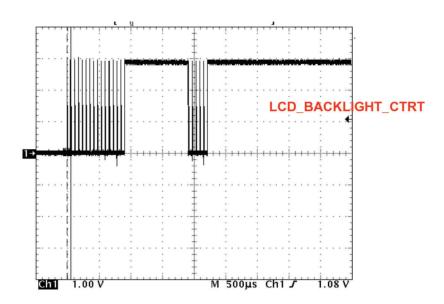
FPCB CONNECTOR



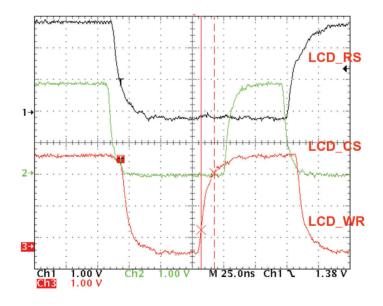
LCD BACKLIGHT



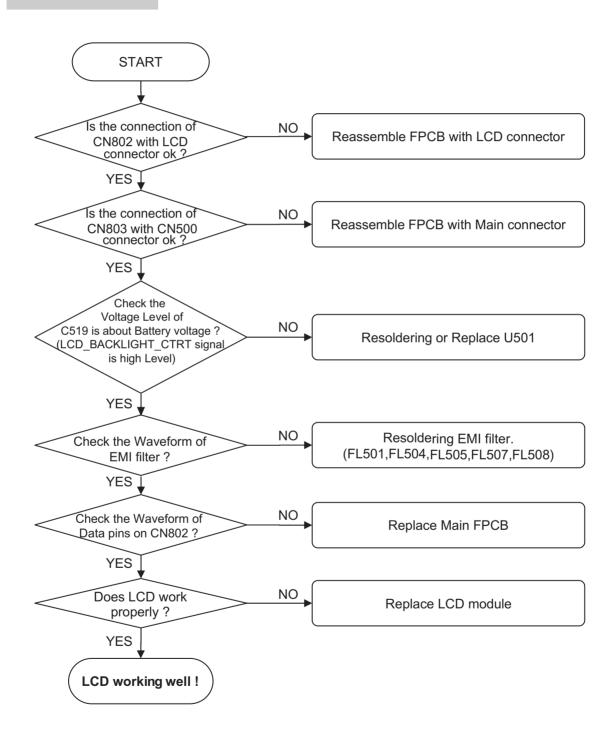
Waveform



Graph 4-7-1. LCD Backlight Control Signal Waveform



Graph 4-7-2. LCD Data Waveform



4.8 Camera Trouble

TEST POINT

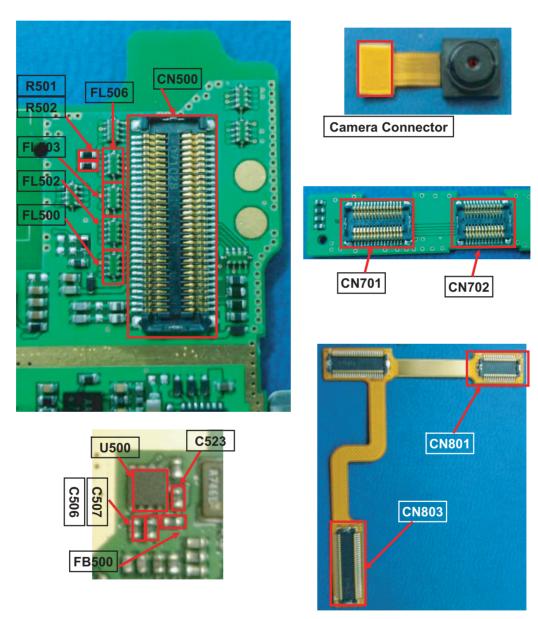
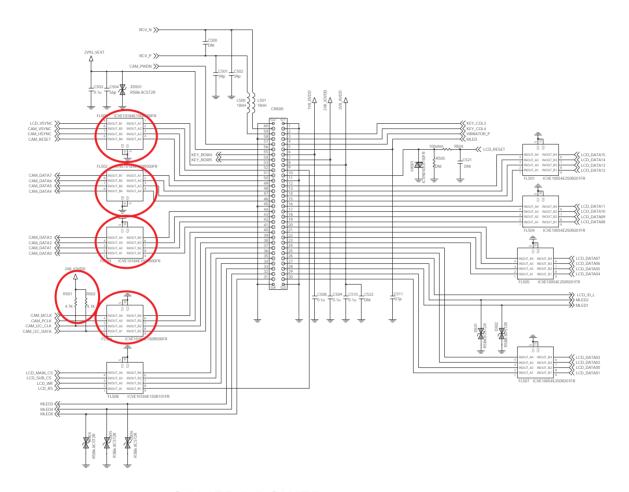


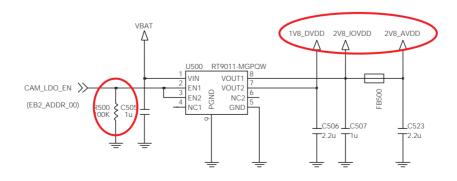
Figure 4-8

CIRCUIT

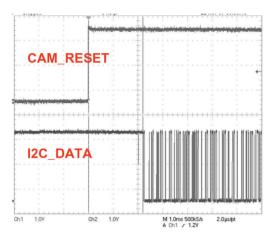
FPCB CONNECTOR



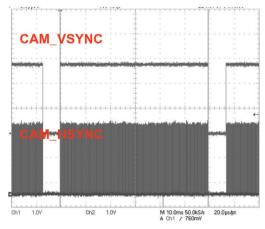
CAMERA POWER



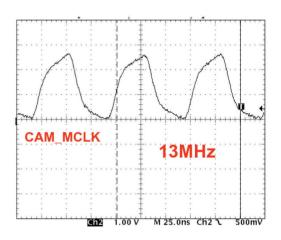
Waveform



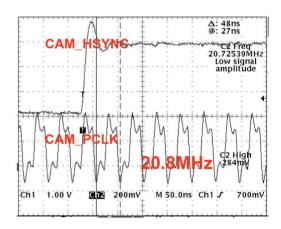
Graph 4-8-1 I2C Data Waveform



Graph 4-8-3 CAM VSYNC vs. CAM HSYNC Waveform

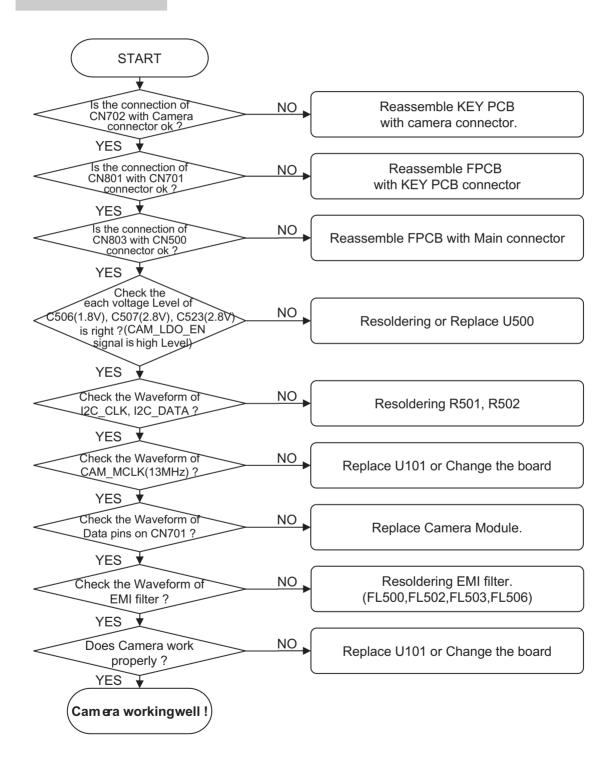


Graph 4-8-2 MCLK Waveform



Graph 4-8-4 CAM HSYNC vs. CAM PCLK Waveform

4. TROUBLE SHOOTING



4.9 Speaker Trouble

TEST POINT

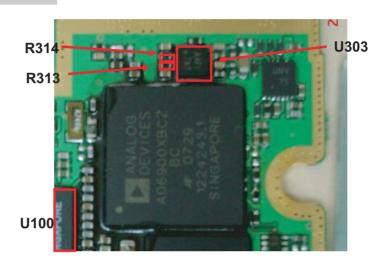
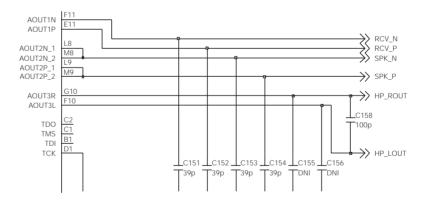
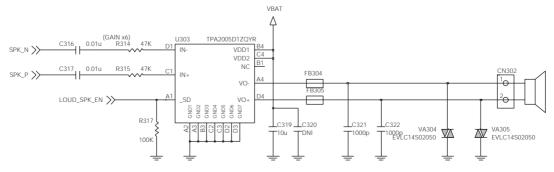


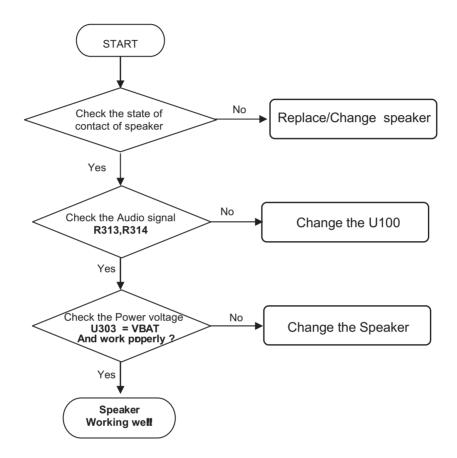
Figure 4-9

CIRCUIT



SPEAKER





4.10 Earphone Trouble

TEST POINT

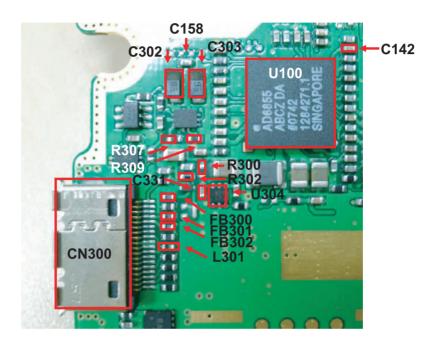
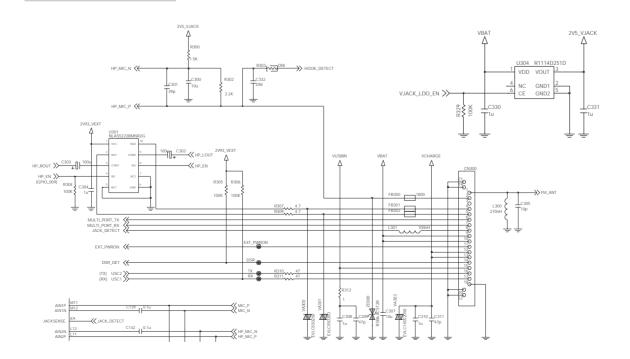
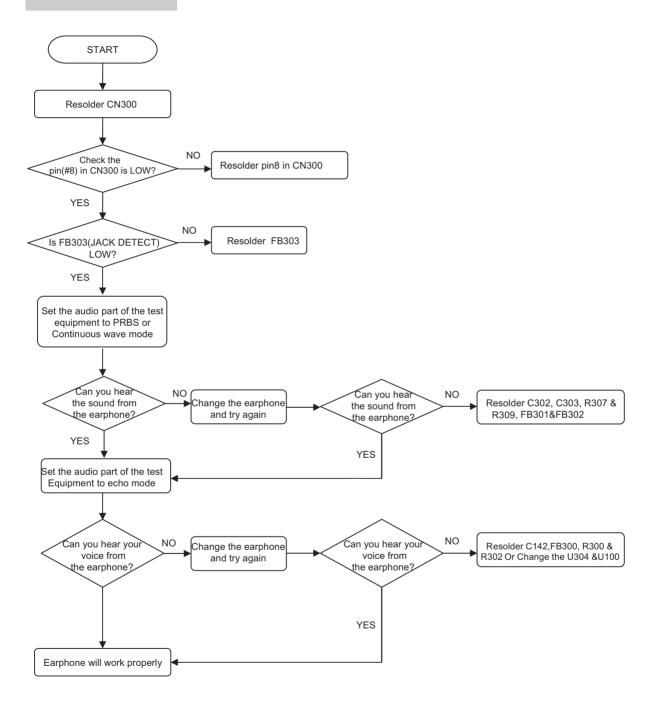


Figure 4-10



4. TROUBLE SHOOTING



4.11 Receiver Trouble

TEST POINT

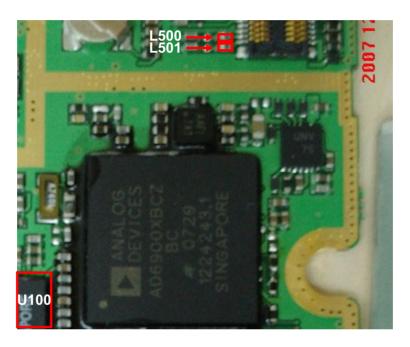
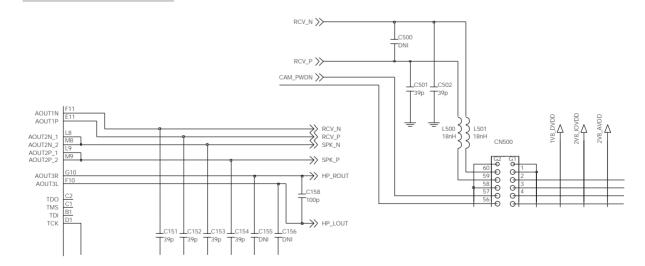


Figure 4-11

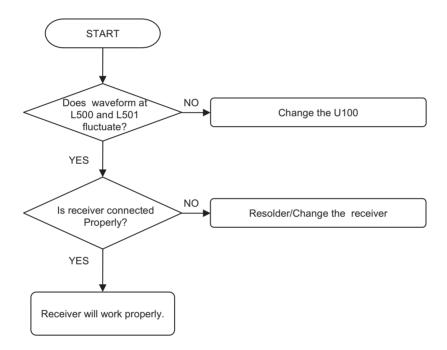


4. TROUBLE SHOOTING

CHECKING FLOW

SETTING: After initialize Agilent 8960, Test GSM850, PCS mode

Set the property of audio as PRBS or continuous wave. Set the receiving volume of mobile as Max.



4.12 Microphone Trouble

TEST POINT

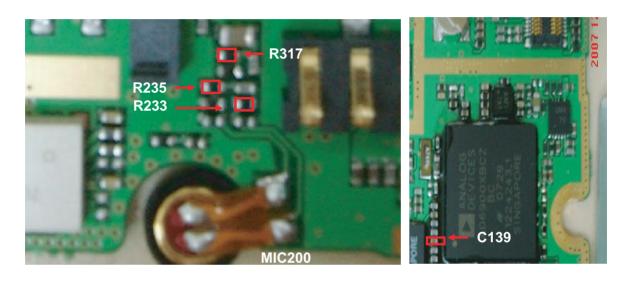
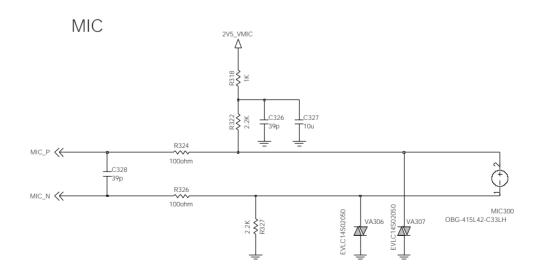
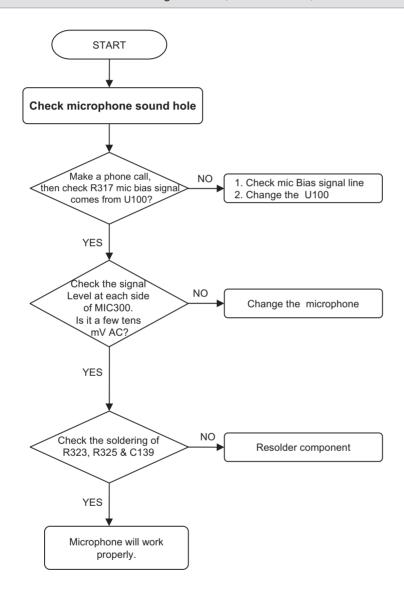


Figure 4-12



SETTING: After initialize Agilent 8960, Test GSM850, PCS mode



4.13 SIM Card Interface Trouble

TEST POINT

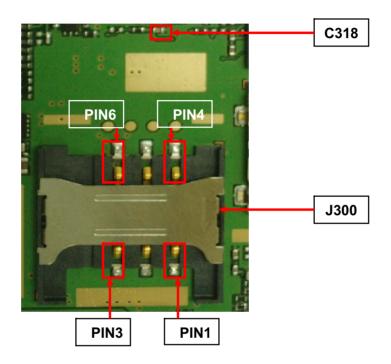
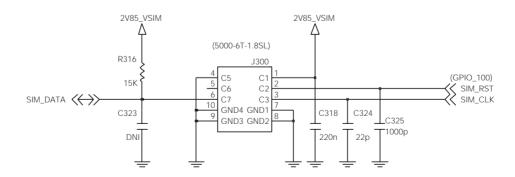
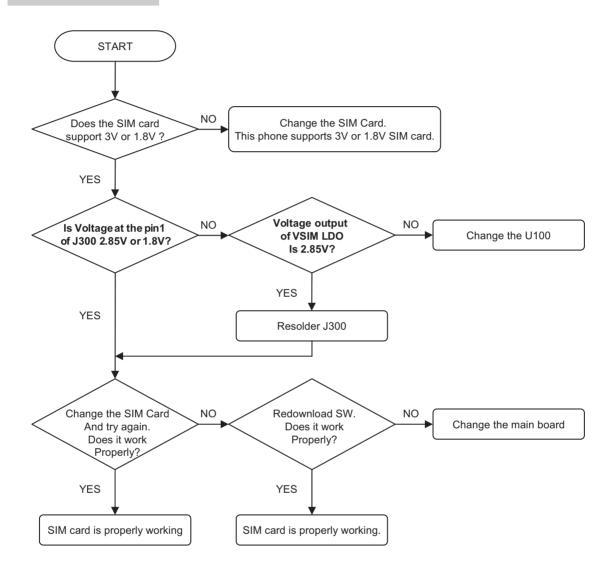


Figure 4-13

TEST POINT

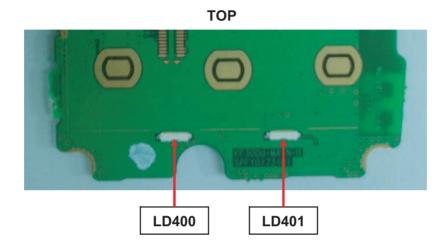


4. TROUBLE SHOOTING



4.14 KEY backlight Trouble

TEST POINT

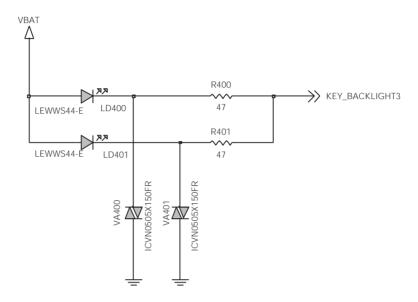


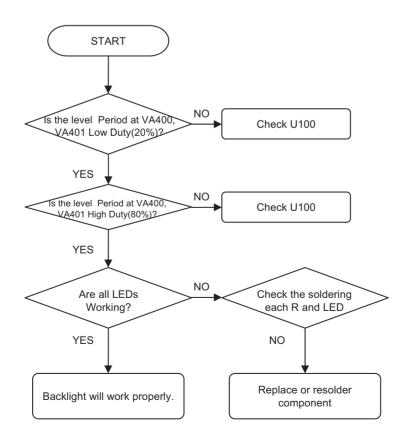
R401 VA401 R400 VA400

Figure 4-14

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CIRCUIT





4.15 RTC Trouble

TEST POINT

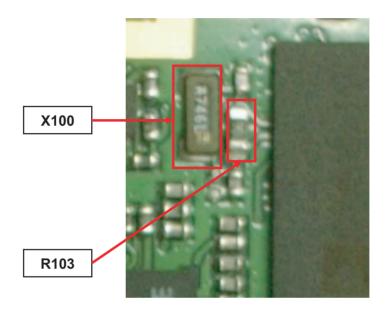
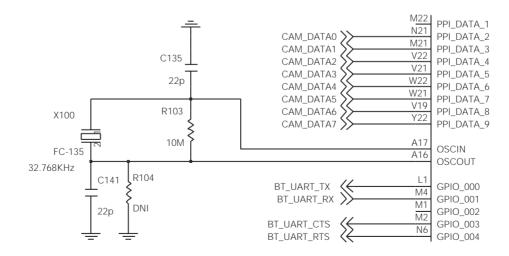
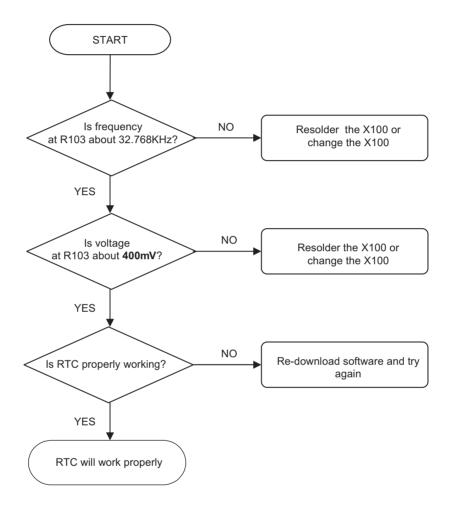


Figure 4-15



CHECK FLOW



4.16 Folder on/off Trouble

TEST POINT

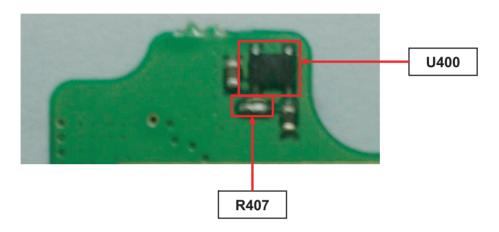
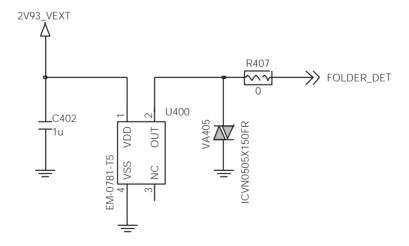
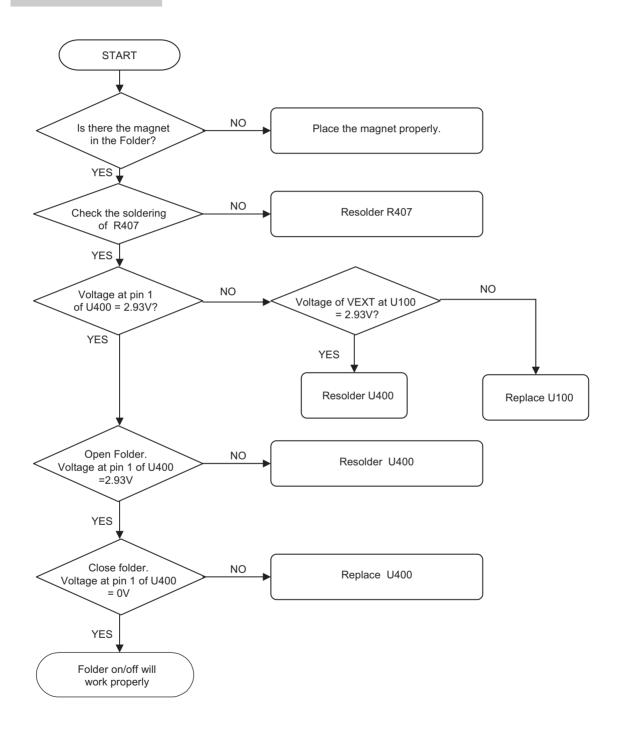


Figure 4-16





4.17 Micro SD Trouble

TEST POINT

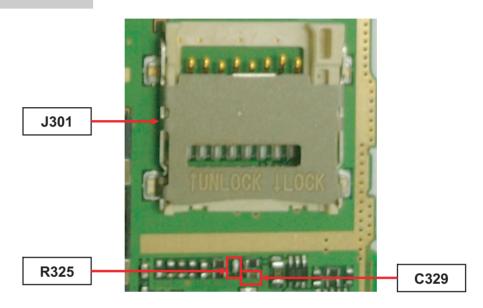
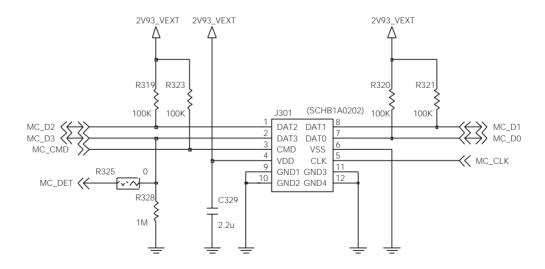
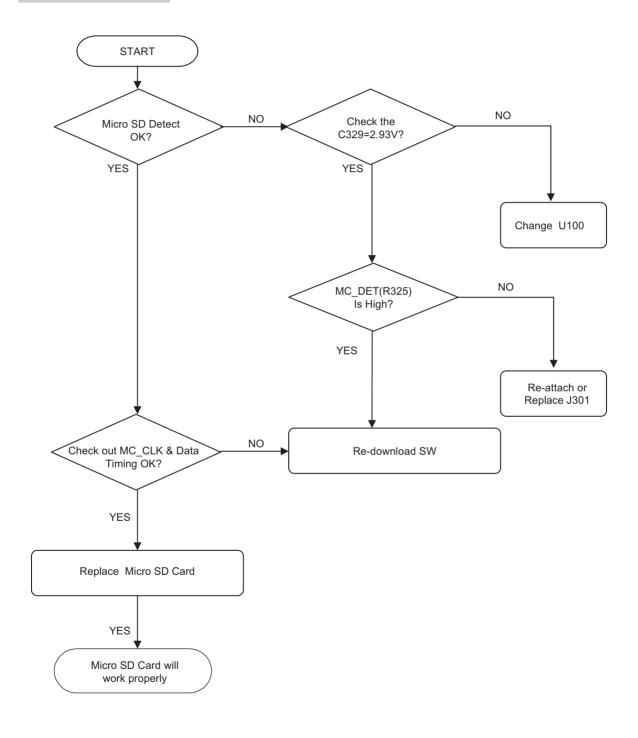


Figure 4-17





4.18 Bluetooth Trouble

TEST POINT

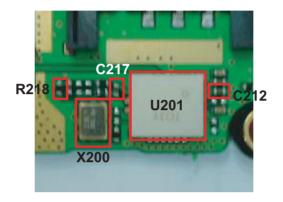
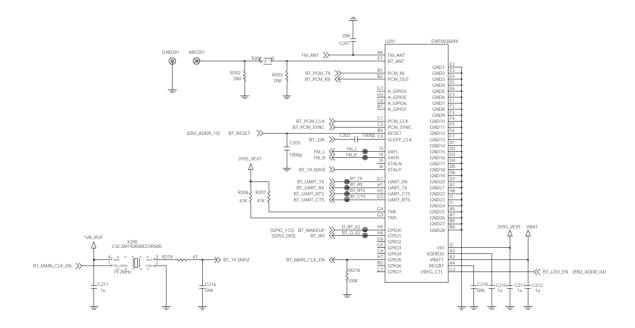
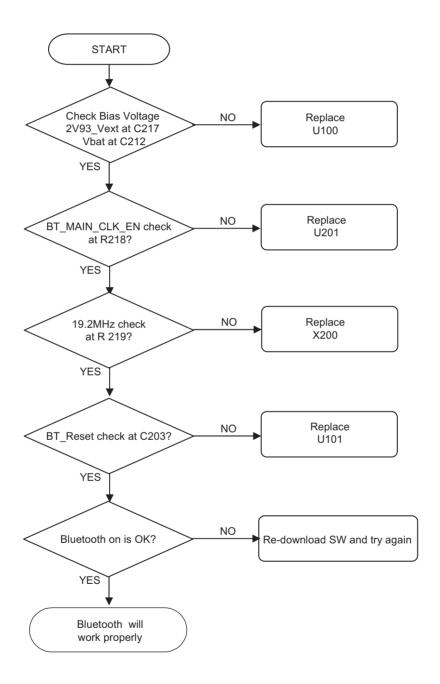


Figure 4-18





4.19 FM Radio Trouble

TEST POINT

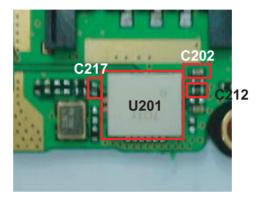
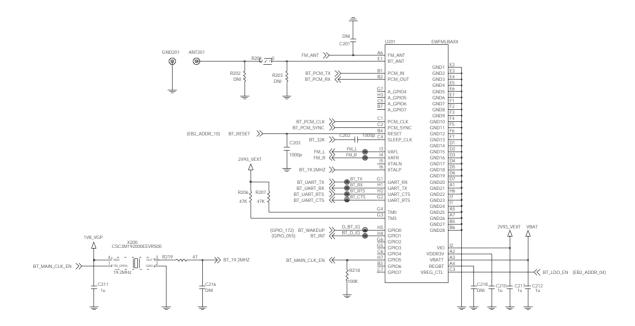
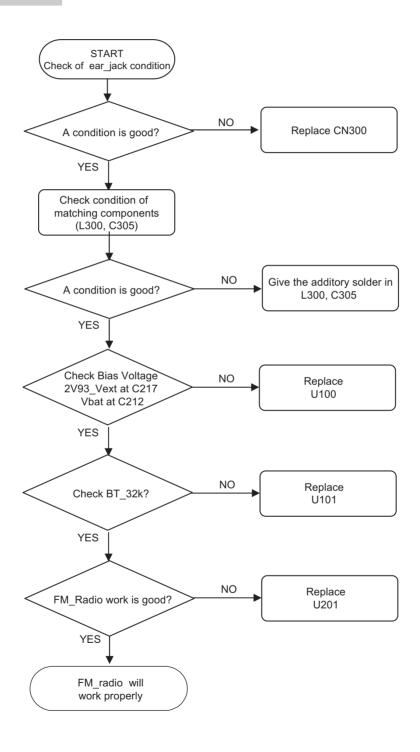


Figure 4-19





5. DOWNLOAD

5.1 Download

A. Download Setup

Figure 5-1 describes Download setupp

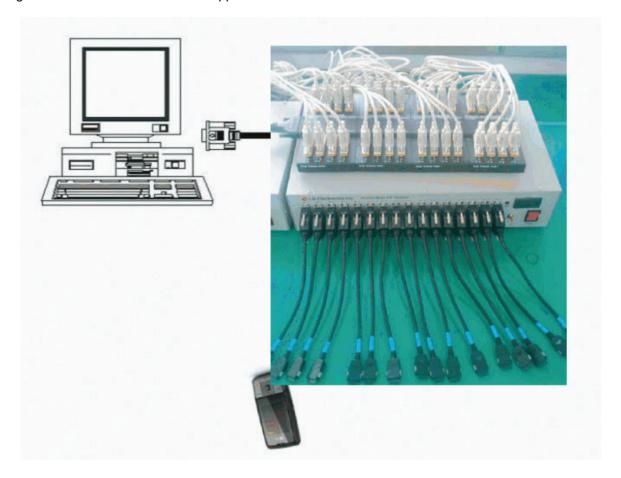
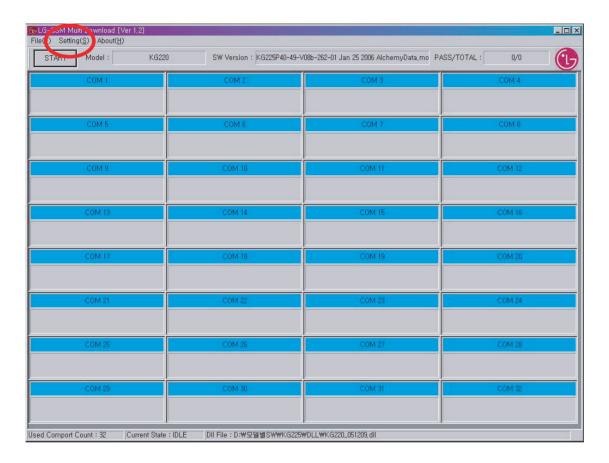


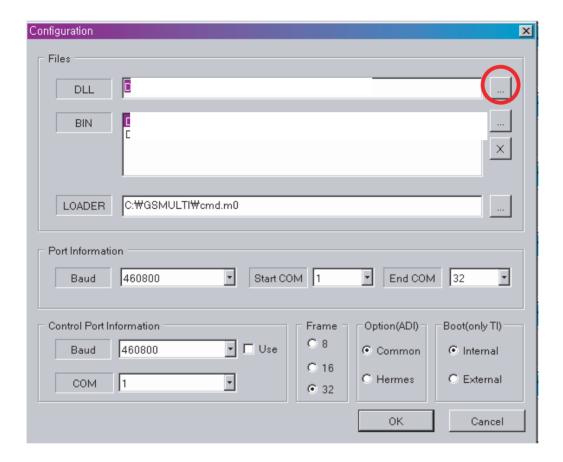
Figure 5-1 Download Setup

B. Multi Download Procedure

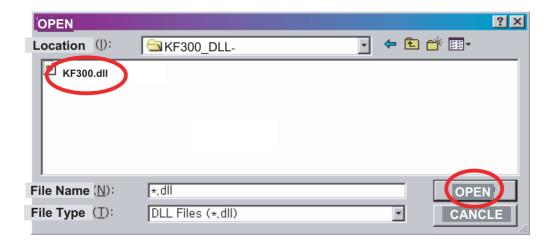
1. Run GSM Multi Download program and select Setting





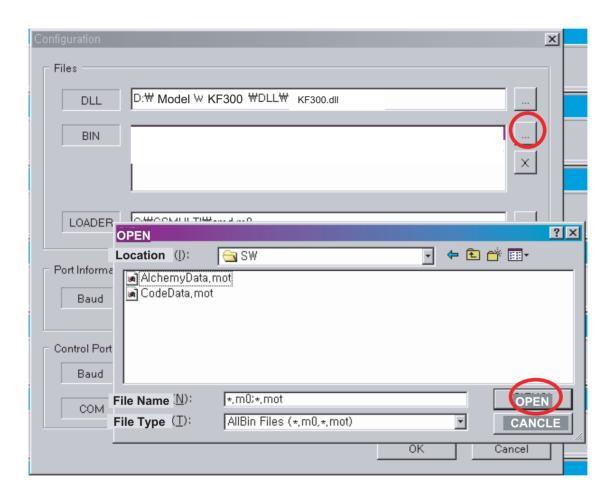


3. Press ... key to select DLL file and press Open

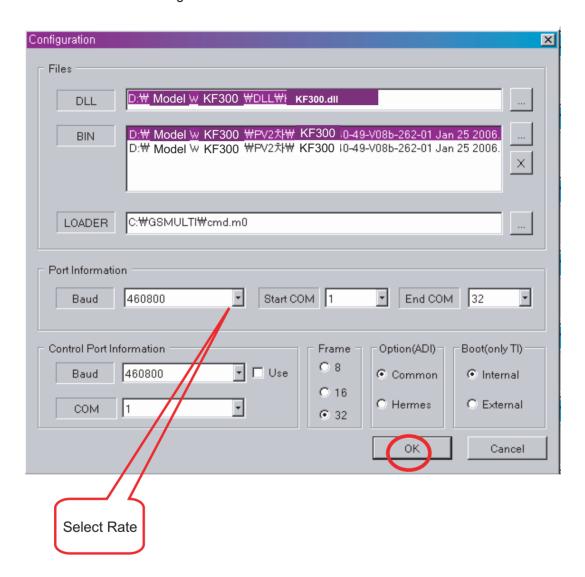


5. DOWNLOAD

- 4. Press ... key to select the mot files
- 5. Select AlchemyData.mot and press open
- 6. Repeat step 4-5 to select CodeData.mot

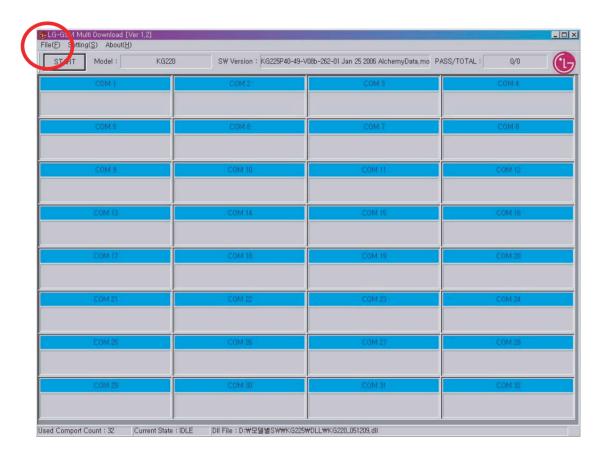


- 7. Check if the ADI option is set to Hermes
- 8. Press OK to end Configuration

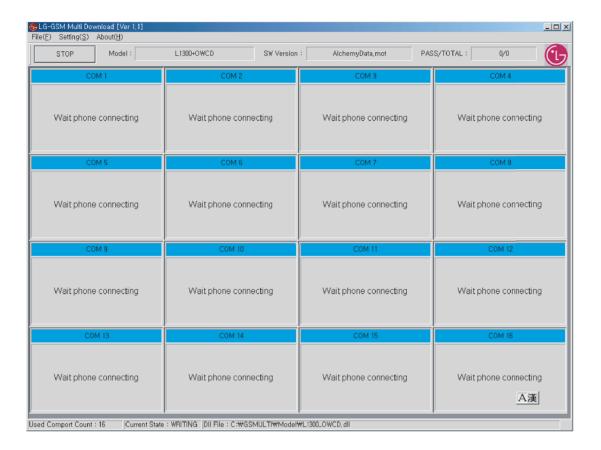


5. DOWNLOAD

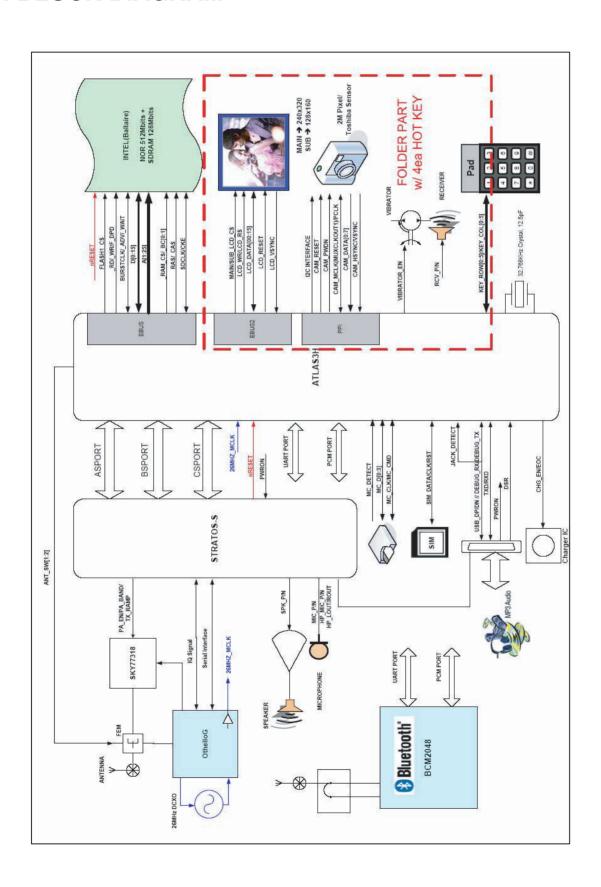
- 9. "Waiting phone connecting" pops up when you pushe the "Start" button in Multi download screen. Then you need to connect the mobile phone with I/O Cable to get downloaded.
- Once downloading is started,
 press STOP button to keep from re-downloading after downloading is completed.

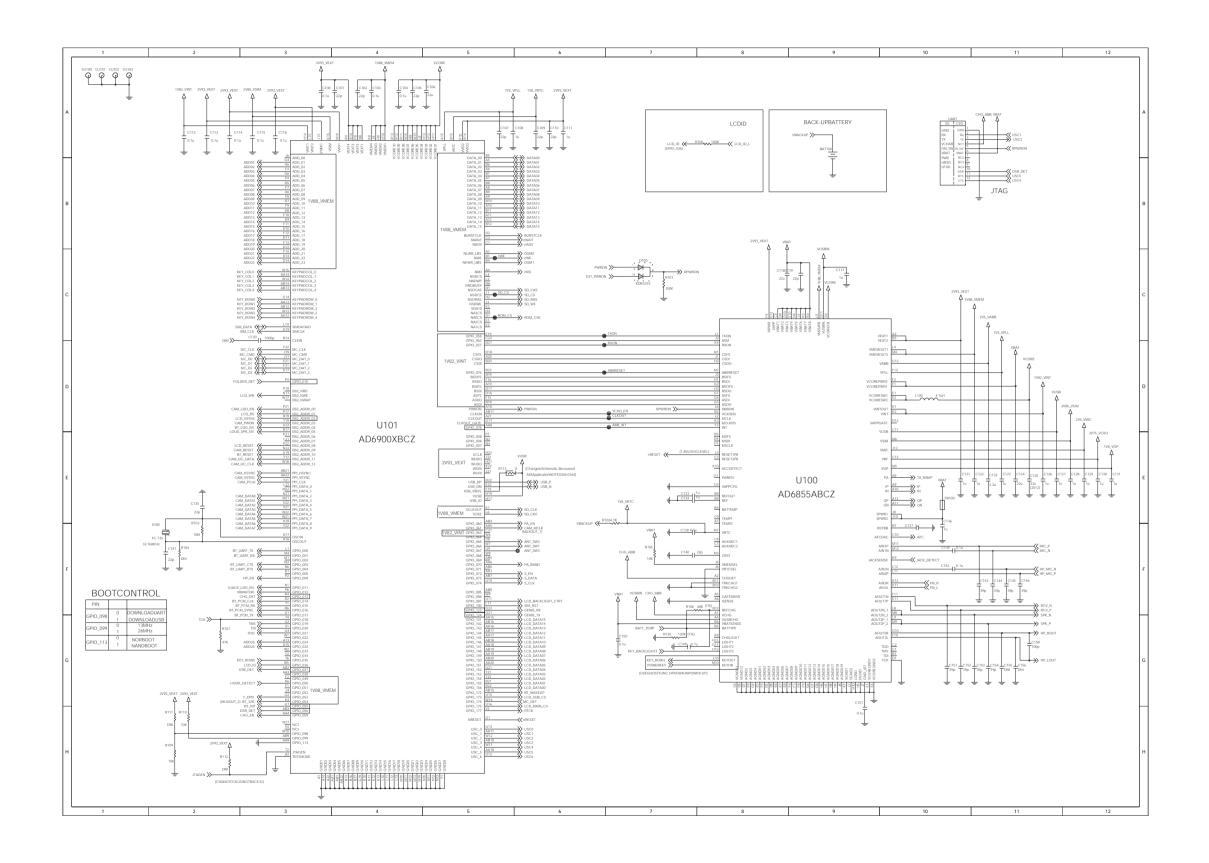


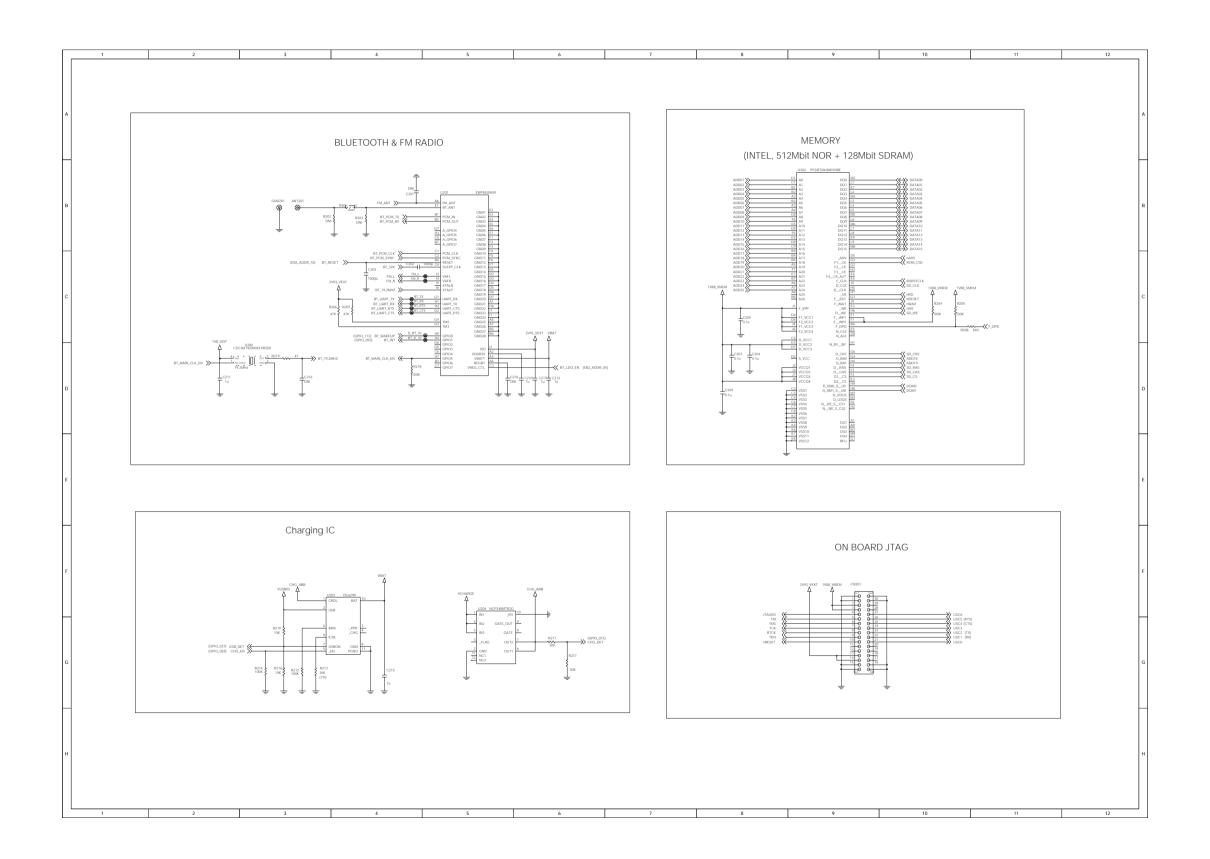


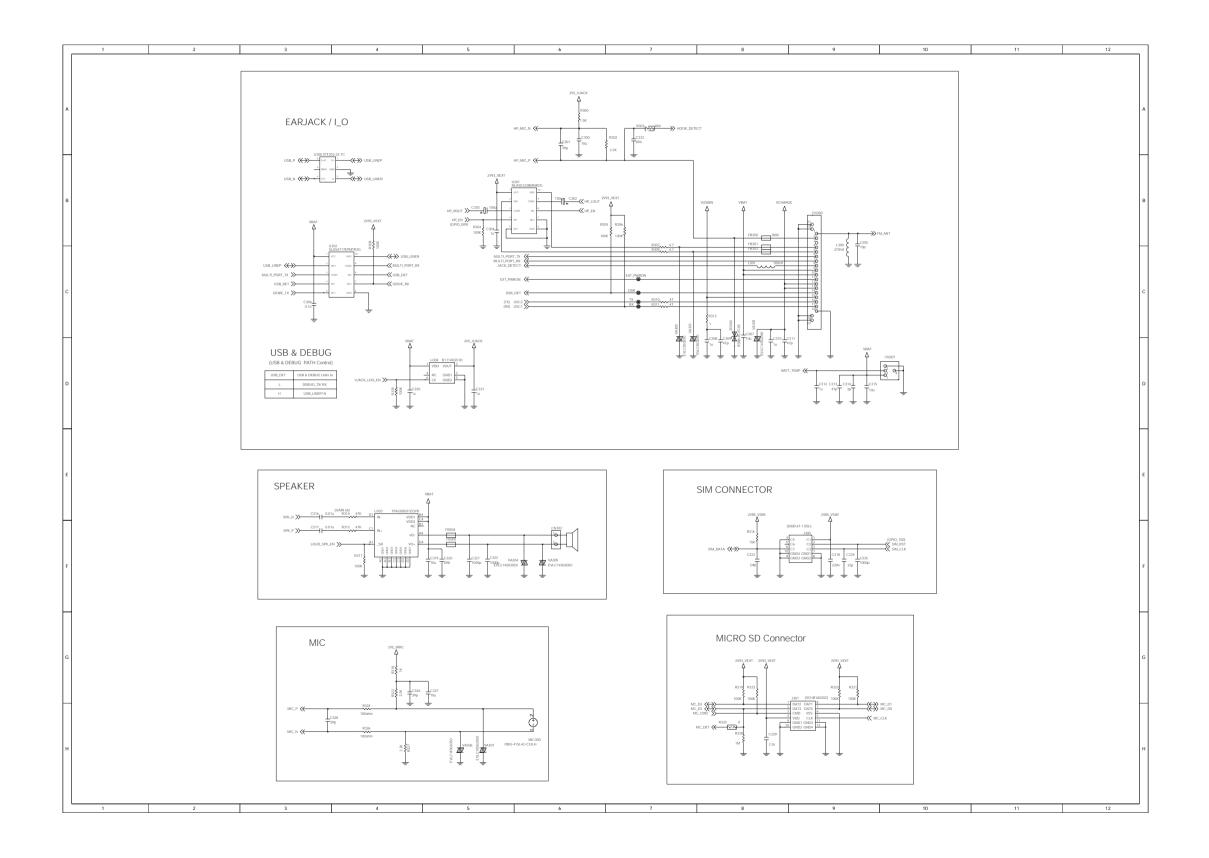


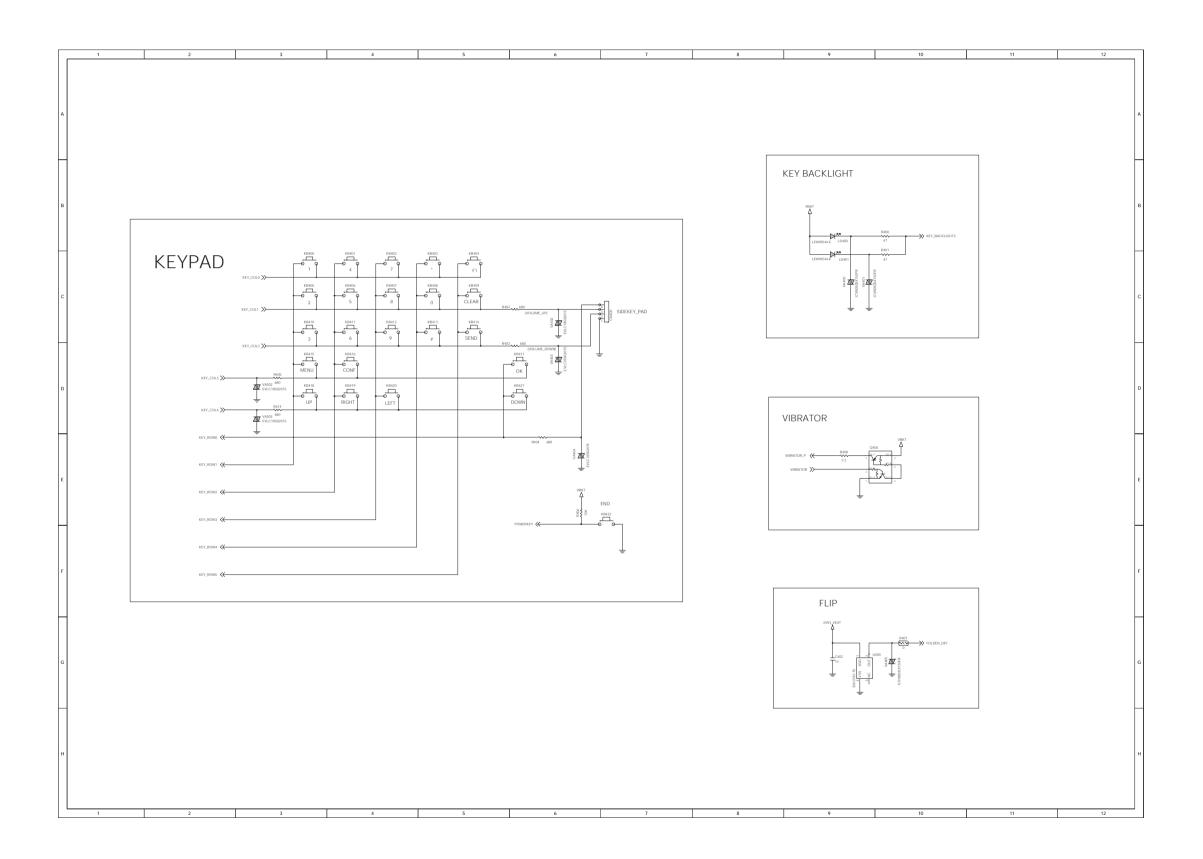
6. BLOCK DIAGRAM

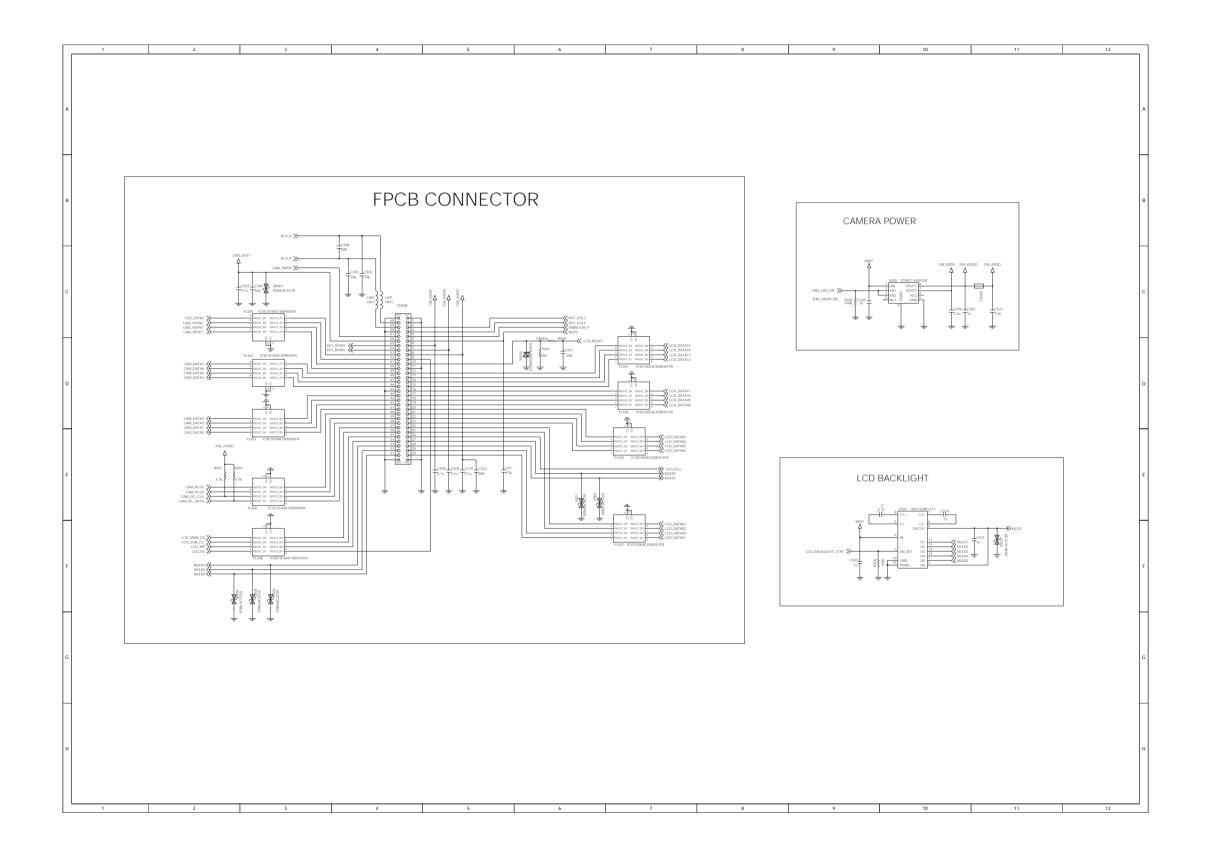


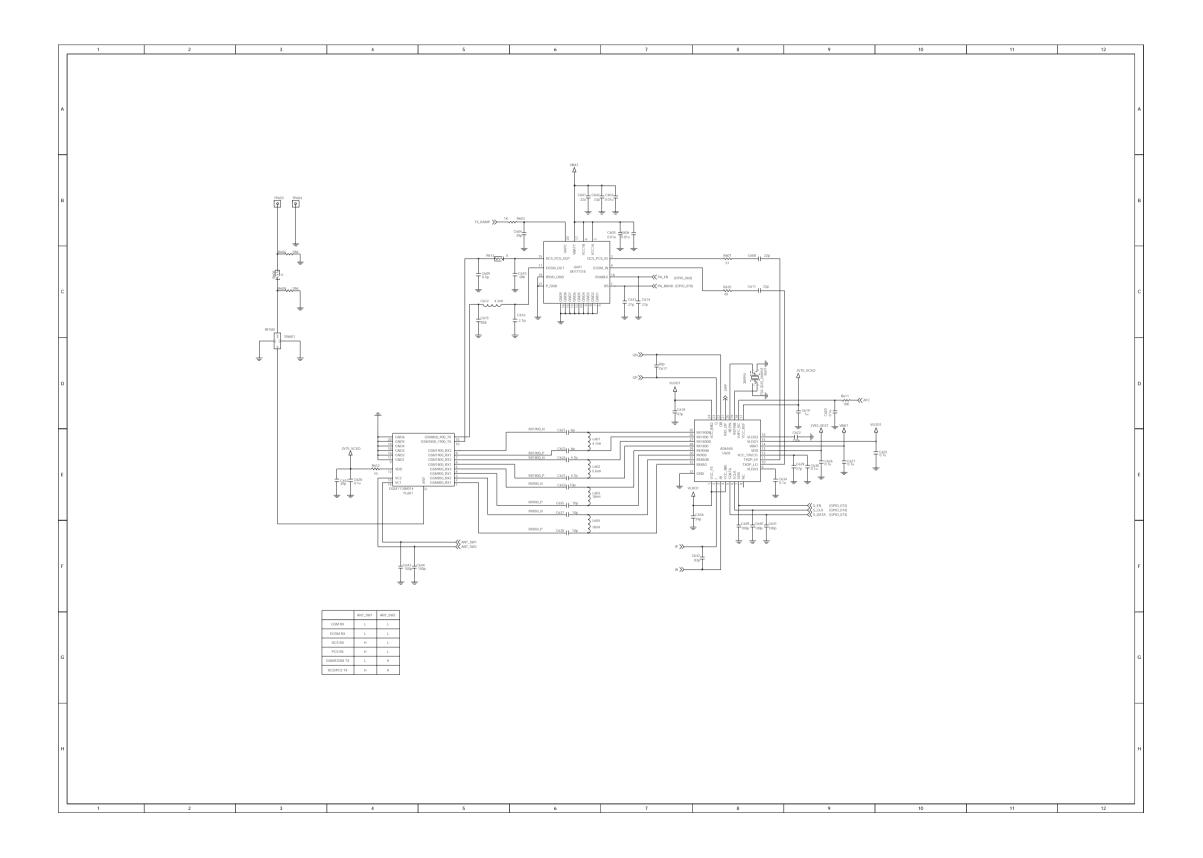


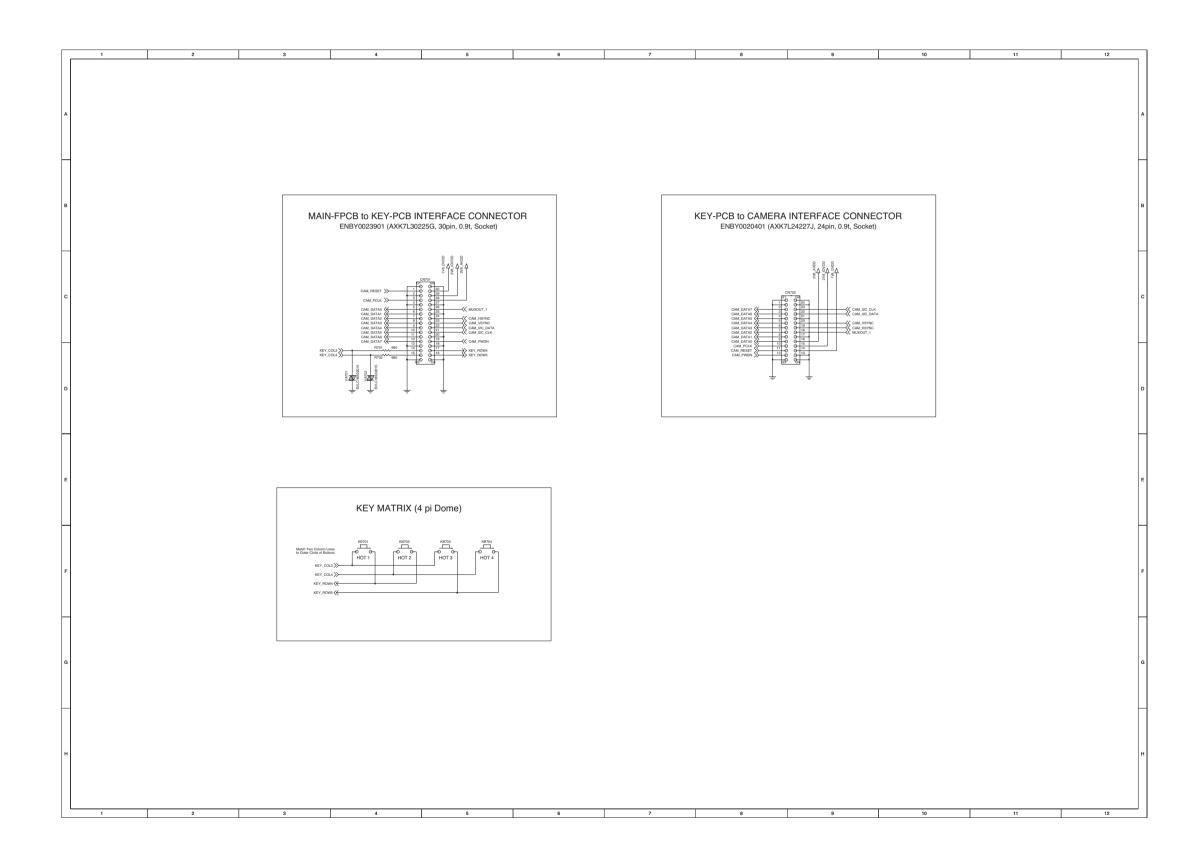


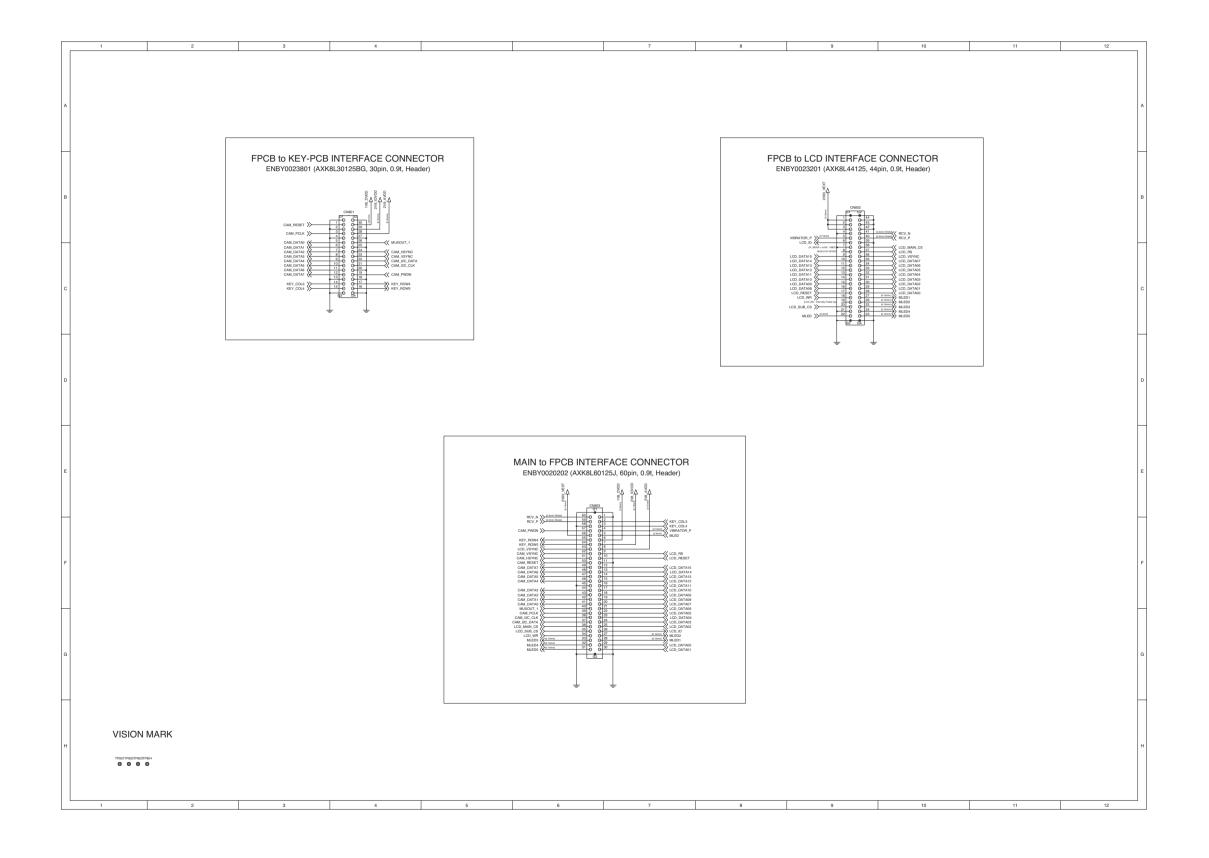


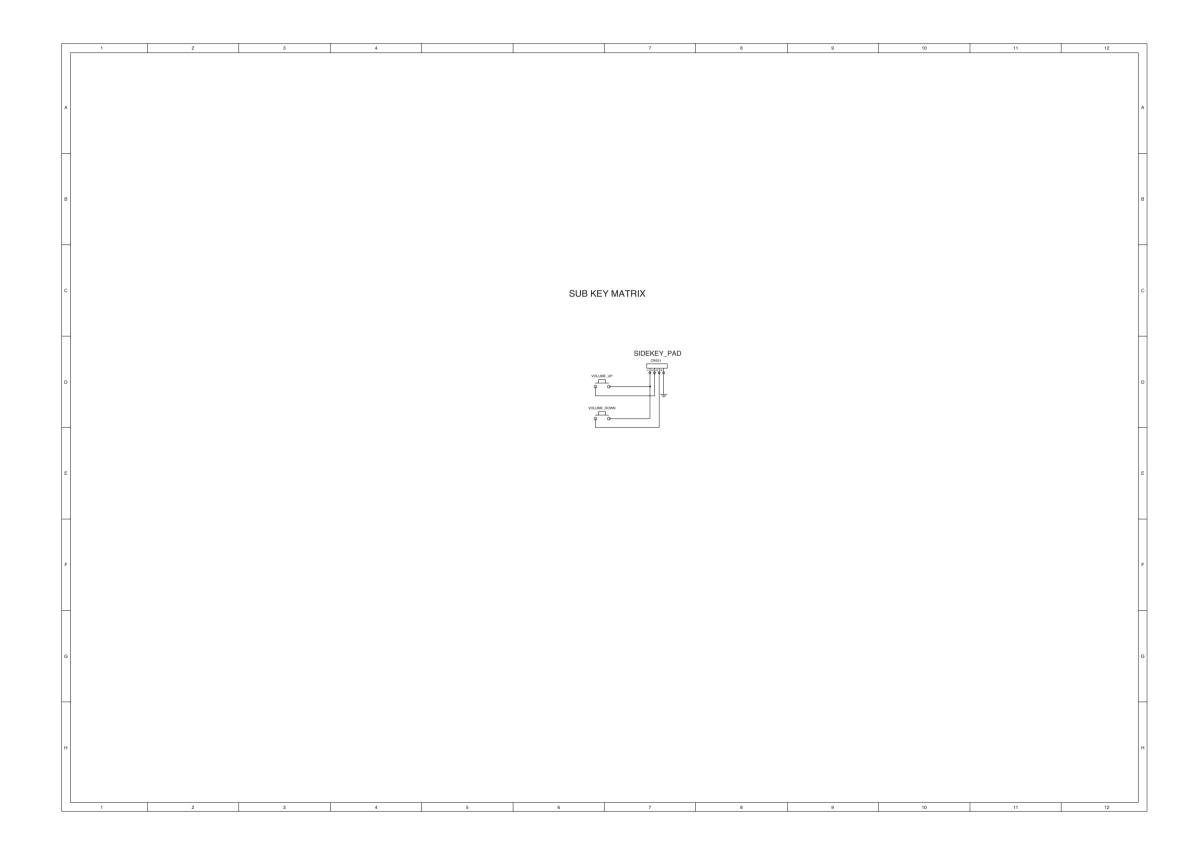






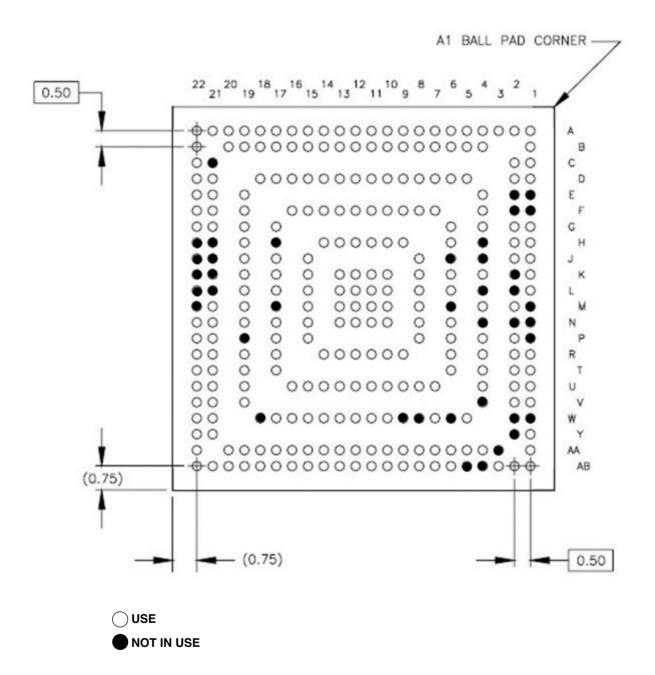




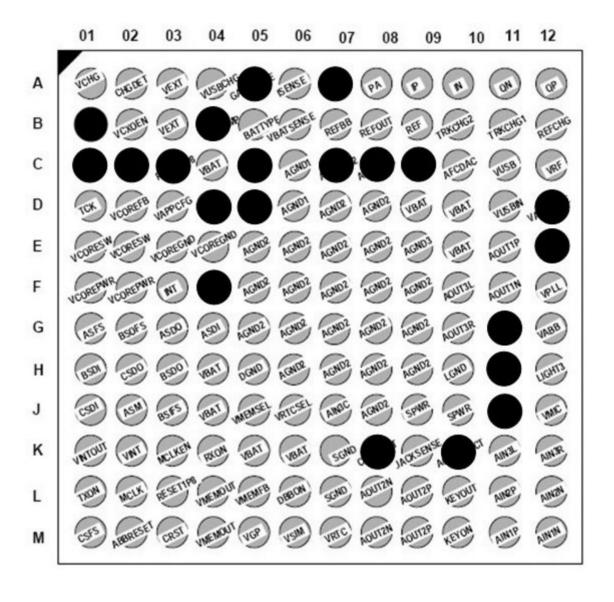


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8. BGA IC Pin Check

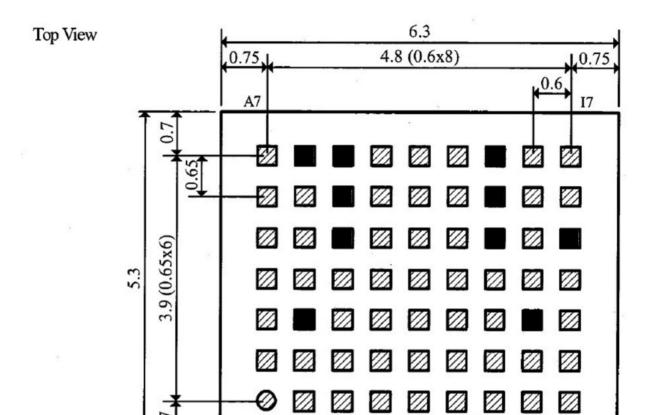


AD6855 Terminal Locations (Top view)



OUSE

NOT IN USE

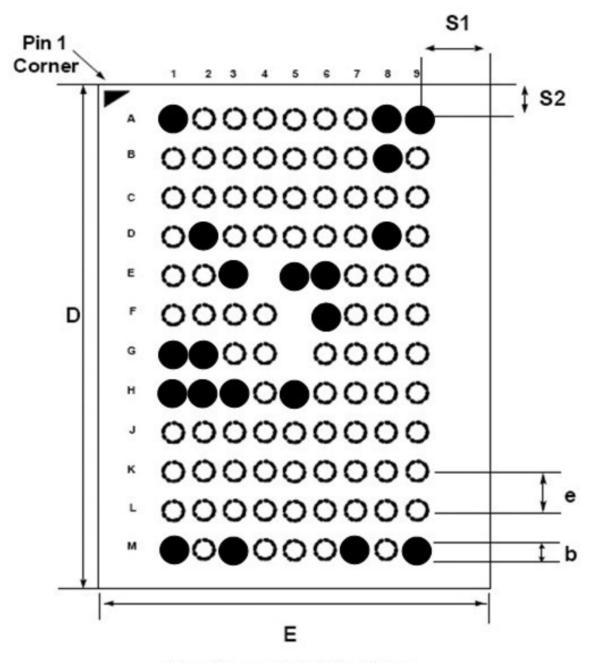


A1

OUSE

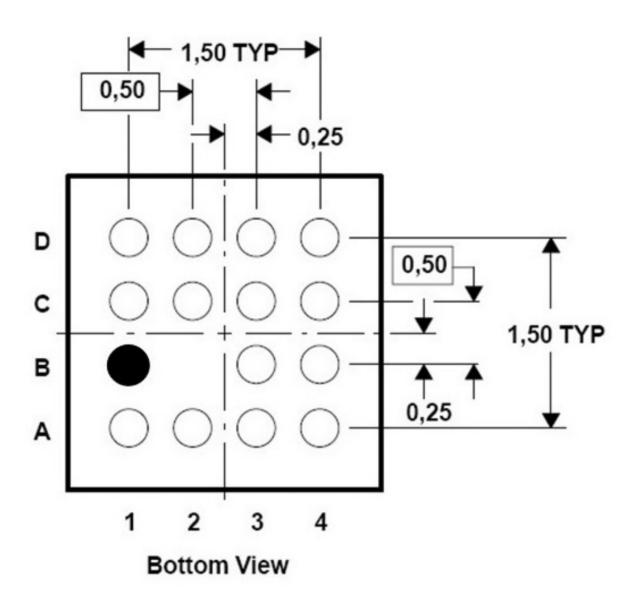
NOT IN USE

I1



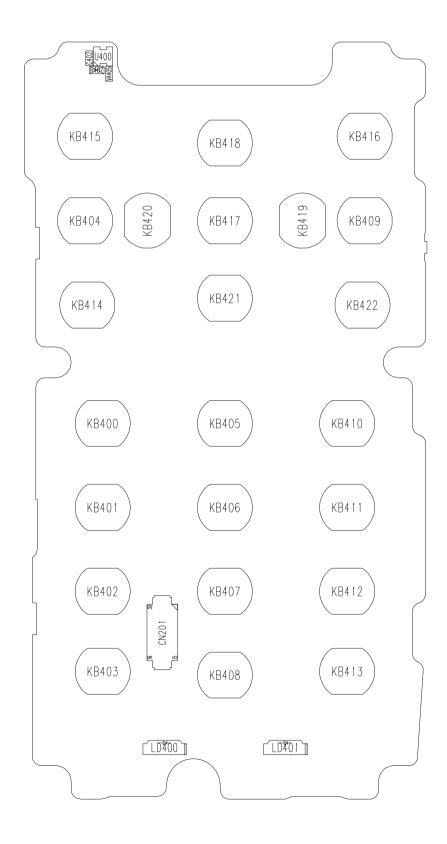
Top View - Ball Side Down

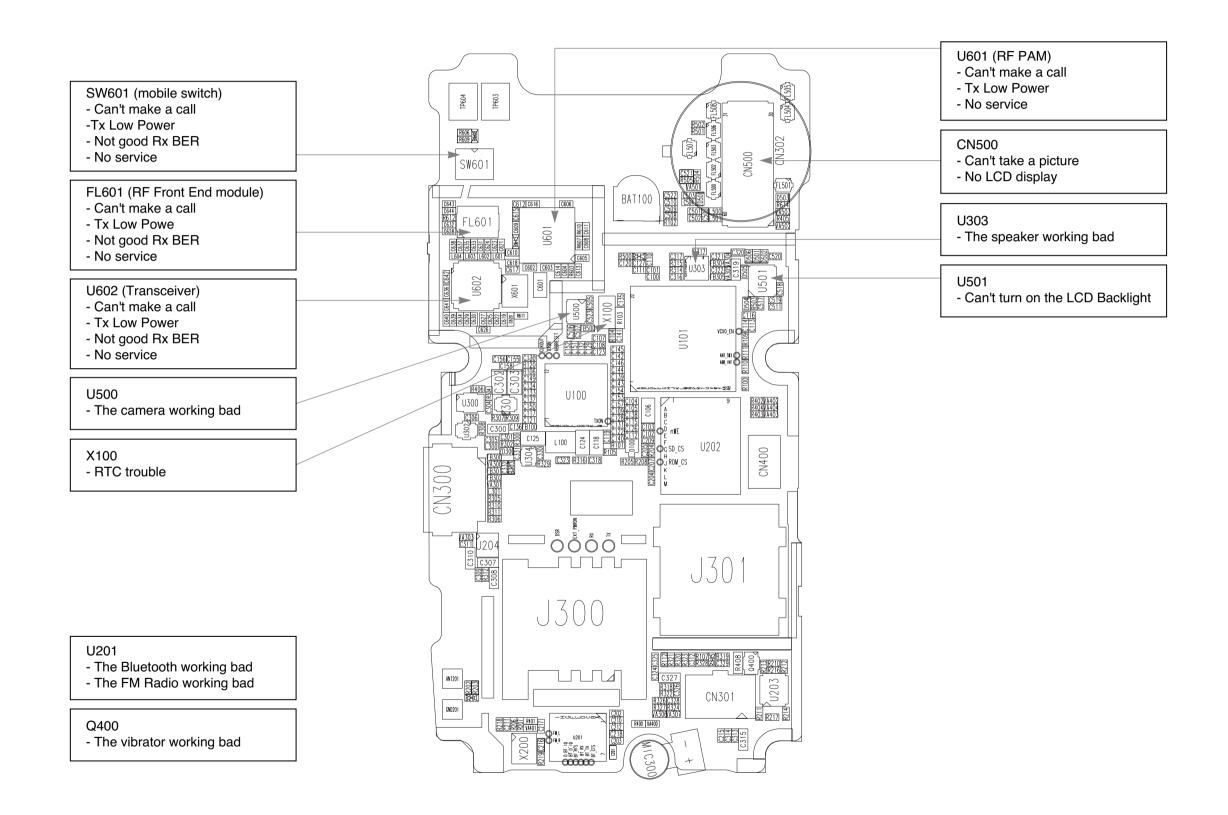
USE NOT IN USE

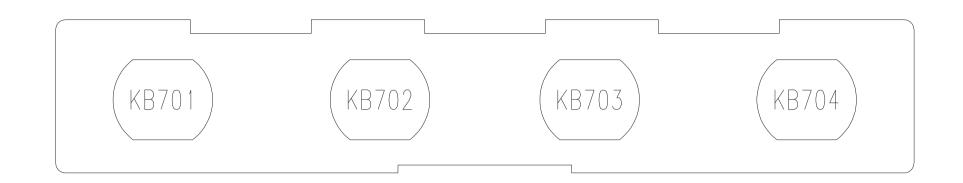


OUSE

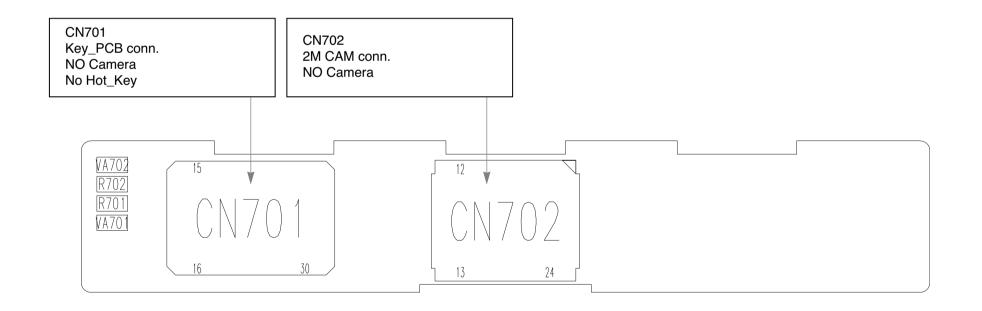
NOT IN USE



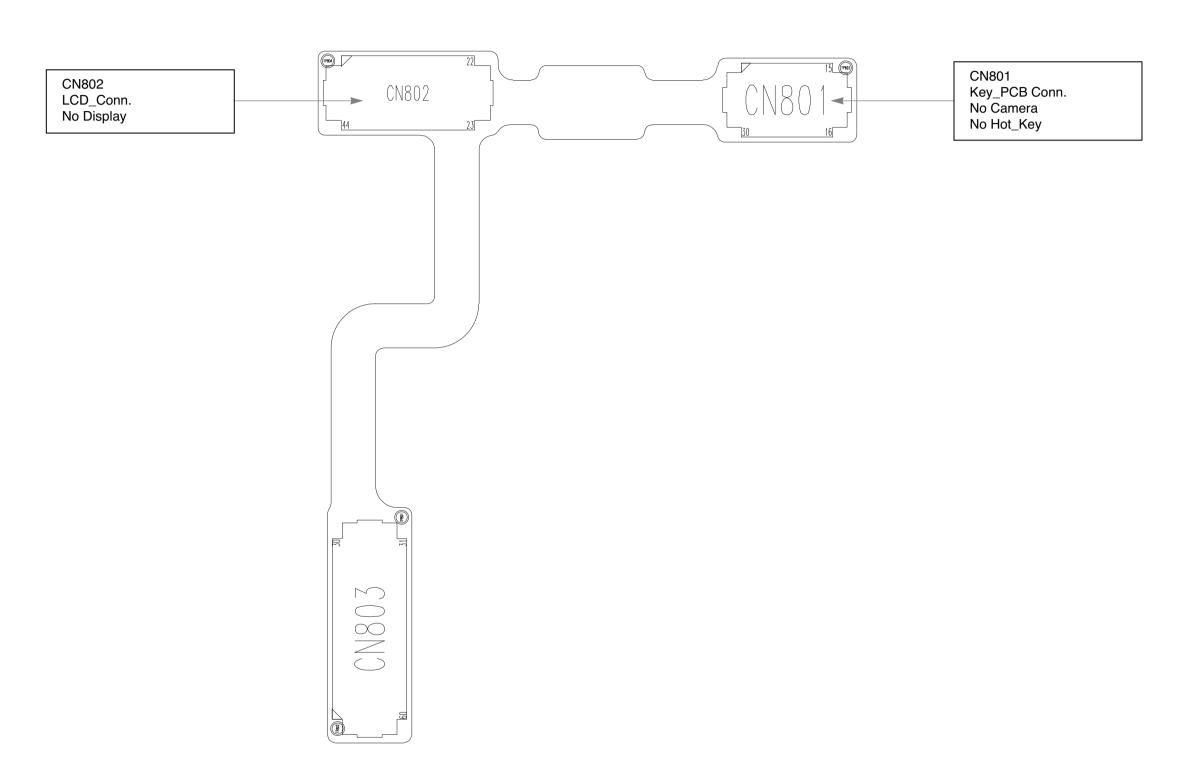




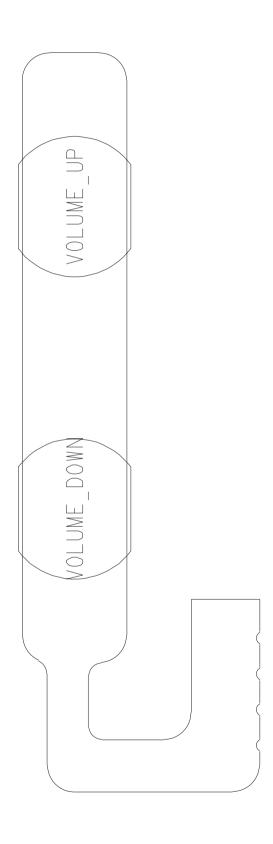
KP300d-H0TKEY-SPEY0054801-1.0-T0P



KP300d-H0TKEY-SPEY0054801-1.0-BTM



KP300d-MAIN-FPCB-SPCY0129001-TOP



10. ENGINEERING MODE

A. About Engineering Mode

Engineering mode is designed to allow a service man/engineer to view and test the basic functions provided by a handset.

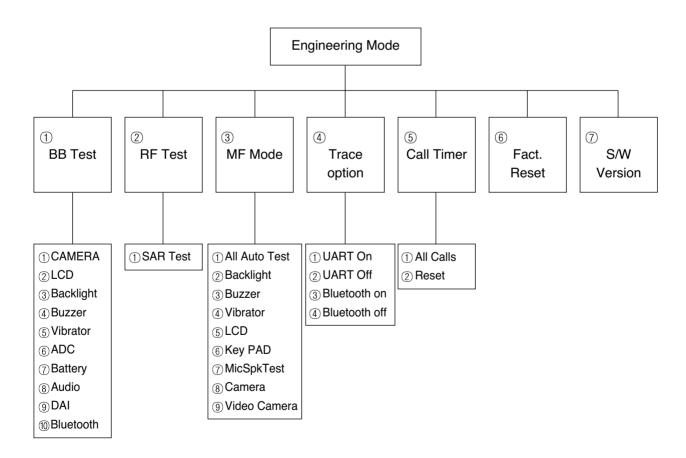
B. Access Codes

The key sequence for switching the engineering mode on is 2945#*#. Pressing END will switch back to non-engineering mode operation.

C. Key Operation

Use Up and Down key to select a menu and press 'select' key to progress the test. Pressing 'back' key will switch back to the original test menu.

D. Engineering Mode Menu Tree



10.1 BB Test [MENU 1]

10.1.1 CAMERA

This menu is to test the Camera.

1) Main LCD preview: It shows the picture on Main LCD.

10.1.2 LCD

1) COLOUR: WHITE, RED, GREEN, BLUE, BLACK

2) Contrast Value

10.1.3 Backlight

This menu is to test the LCD Backlight and Keypad EL Backlight.

- 1) Backlight on: LCD Backlight and Keypad EL Backlight light on at the same time.
- 2) Backlight off: LCD Backlight and Keypad EL Backlight light off at the same time.
- 3) Backlight value: This controls brightness of Backlight. When entering into the menu,the present backlight-value in the phone is displayed. Use Left/Right key to adjust the level of brightness. The value of the brightness set at last will be saved in the NVRAM.

10.1.4 Buzzer

This menu is to test the melody sound.

- 1) Melody on : Melody sound is played through the speaker.
- 2) Melody off: Melody sound is off.

10.1.5 Vibrator

This menu is to test the vibration mode.

- 1) Vibrator on: Vibration mode is on.
- 2) Vibrator off: Vibration mode is off.

10.1.6 ADC (Analog to Digital Converter)

This displays the value of each ADC.

1) MVBAT ADC: Main Voltage Battery ADC

2) AUX ADC: Auxiliary ADC

3) TEMPER ADC: Temperature ADC

10.1.7 BATTERY

 Bat Cal: This displays the value of Battery Calibration. The following menus are displayed in order: BAT_LEV_4V, BAT_LEV_3_LIMIT, BAT_LEV_2_LIMIT, BAT_LEV_1_LIMIT, BAT_IDLE_LI MIT, BAT_INCALL_LIMIT, SHUT DOWN VOLTAGE, BAT RECHARGE LMT

2) TEMP Cal: This displays the value of Temperature Calibration. The following menus are displayed in order: TEMP_HIGH_LIMIT, TEMP_HIGH_RECHARGE_LMT, TEMP_LOW_RECHARGE_LMT, TEMP_LOW_LIMIT

10.1.8 Audio

This is a menu for setting the control register of Voiceband Baseband Codec chip.

Although the actual value can be written over, it returns to default value after switching off and on the phone.

1) VbControl1: VbControl1 bit Register Value Setting

2) VbControl2: VbControl2 bit Register Value Setting

3) VbControl3: VbControl3 bit Register Value Setting

4) VbControl4: VbControl4 bit Register Value Setting

5) VbControl5: VbControl5 bit Register Value Setting

6) VbControl6: VbControl6 bit Register Value Setting

9.1.9 DAI (Digital Audio Interface)

This menu is to set the Digital Audio Interface Mode for Speech Transcoder and Acoustic testing.

1) DAI AUDIO: DAI audio mode

2) DAI UPLINK : Speech encoder test3) DAI DOWNLINK : Speech decoder test

4) DAI OFF: DAI mode off

10.2 RF Test [MENU 2]

10.2.1 SAR test

This menu is to test the Specific Absorption Rate.

- 1) SAR test on: Phone continuously process TX only. Call-setup equipment is not required.
- 2) SAR test off: TX process off

10.3 MF mode [MENU 3]

This manufacturing mode is designed to do the baseband test automatically. Selecting this menu will process the test automatically, and phone displays the previous menu after completing the test.

10.3.1 All auto test

LCD, Backlight, Vibrator, Buzzer, Key Pad, Mic&Speaker,

10.3.2 Backlight

LCD Backlight is on for about 1.5 seconds at the same time, then off.

10.3.3 Buzzer

This menu is to test the volume of Melody. It rings in the following sequence. Volume 1, Volume 2, Volume 3, Volume 0 (mute), Volume 4, Volume 5.

10.3.4 Vibrator

Vibrator is on for about 1.5 seconds.

10.3.5 LCD

1)LCD

Main LCD screen resolution tests horizontally and vertically one by one and fills the screen.

10.3.6 Key pad

When a pop-up message shows °ÆPress Any Key°Ø, you may press any keys including side keys, but not [Soft2 Key]. If the key is working properly, name of the key is displayed on the screen. Test will be completed in 15 seconds automatically.

10.3.7 MicSpk Test

The sound from MIC is recorded for about 3 seconds, then it is replayed on the speaker automatically.

10.3.8 Camera Test

This menu is to test camera(preview and capture automatically)

10.4 Trace option [MENU 4]

This is NOT a necessary menu to be used by neither engineers nor users.

10.5 Call timer [MENU 5]

This menu is to set the Digital Audio Interface Mode for Speech Transcoder and Acoustic testing.

- 1) All calls: This displays total conversation time. User cannot reset this value.
- 2) Reset settings: This resets total conversation time to this, [00:00:00].

10.6 Fact. Reset [MENU 6]

This Factory Reset menu is to format data block in the flash memory and this procedure set up the default value in data block.

Attention

- ① Fact. Reset (i.e. Factory Reset) should be only used during the Manufacturing process.
- ② Servicemen should NOT progress this menu, otherwise some of valuable data such as Setting value, RF Calibration data, etc. cannot be restored again.

10.7 S/W version

This displays software version stored in the phone.

11. STAND ALONE TEST

11.1 Introduction

This manual explains how to examine the status of RX and TX of the model.

A. Tx Test

TX test - this is to see if the transmitter of the phones is activating normally.

B. Rx Test

RX test - this is to see if the receiver of the phones is activating normally.

11.2 Setting Method

A. COM port

- a. Move your mouse on the 'Connect' button, then click the right button of the mouse and select "Comsetting'.
- b. In the "Dialog Menu", select the values as explained below.
 - Port : select a correct COM port
 - Baud rate: 38400
 - Leave the rest as default values

B. Tx

- 1. Selecting Channel
 - Select one of GSM or DCS Band and input appropriate channel.
- 2. Selecting APC
 - a. Select either Power level or Scaling Factor.
 - b. Power level
 - Input appropriate value GSM (between 5 ~19) or DCS (between 0 ~15)
 - c. Scaling Factor
 - A 'Ramp Factor' appears on the screen.
 - You may adjust the shape of the Ramp or directly input the values.

C. Rx

- 1. Selecting Channel
 - Select one of GSM or DCS Band and input appropriate channel.
- 2. Gain Control Index (0 ~ 26) and RSSI level
 - See if the value of RSSI is close to -16dBm when setting the value between 0 \sim 26 in Gain Control Index.
 - Normal phone should indicate the value of RSSI close to -16dBm.

11.3 Means of Test

- a. Select a COM port
- b. Set the values in Tx or Rx
- c. Select band and channel
- d. After setting them all above, press connect button.
- e. Press the start button

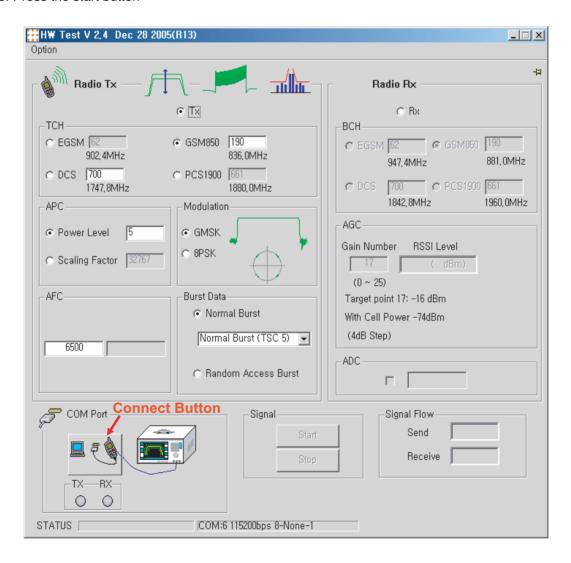
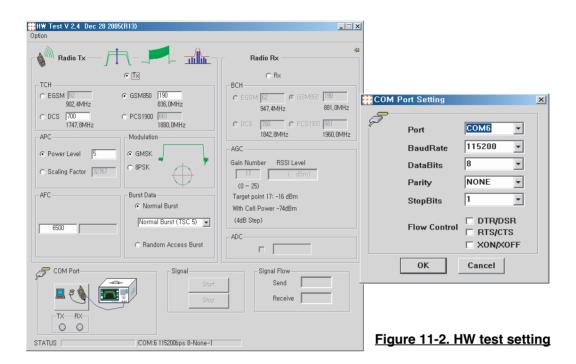
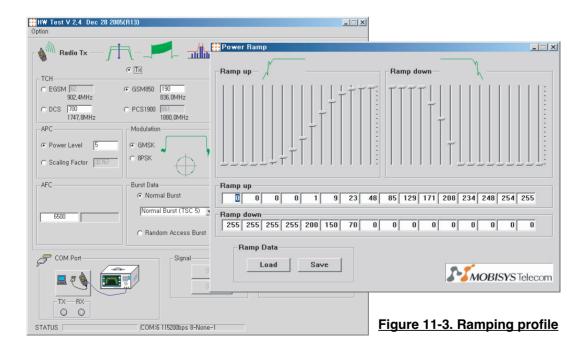


Figure 11-1. HW test program





12. AUTO CALIBRATION

12.1 Overview

Auto-cal (Auto Calibration) is the PC side Calibration tool that perform Tx, Rx and Battery Calibration with Agilent 8960(GSM call setting instrument) and Tektronix PS2521G(Programmable Power supply). Auto-cal generates calibration data by communicating with phone and measuring equipment then write it into calibration data block of flash memory in GSM phone.

12.2 Equipment List

Equipment for Calibration	Type / Model	Brand
Wireless Communication Test Set	HP-8960	Agilent
RS-232 Cable and Test JIG		LG
RF Cable		LG
Power Supply	HP-66311B	Agilent
GPIO interface card	HP-GPIB	Agilent
Calibration & Final test software		LG
Test SIM Card		
PC (for Software Installation)	Pentium II class above 300MHz	

Table 12-2-1. Calibration Equipment List.

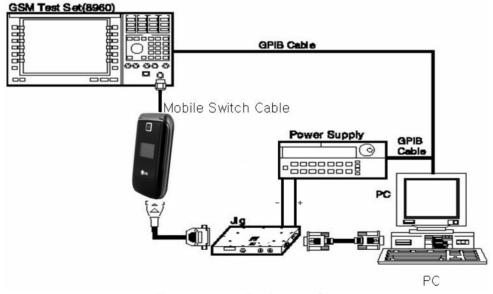


Figure 12-2-2. Equipment Setup

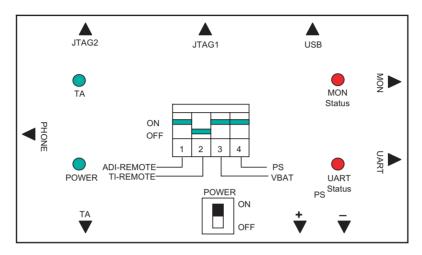


Figure 12-2-3 The top view of Test JIG

12.3 Test Jig Operation

Power Source	Description
Power Supply	Usually 4.2V

Table 12-3-1 Jig Power

Switch Number	Name	Description
Switch 1	ADI-REMOTE	In ON state, phone is awaked. It is used ADI chipset.
Switch 2	TI-REMOTE	In ON state, phone is awaked. It is used TI chipset.
Switch 3	VBAT	Power is provided for phone from battery
Switch 4	PS	Power is provided for phone from Power supply

Table 12-3-2 Jig DIP Switch

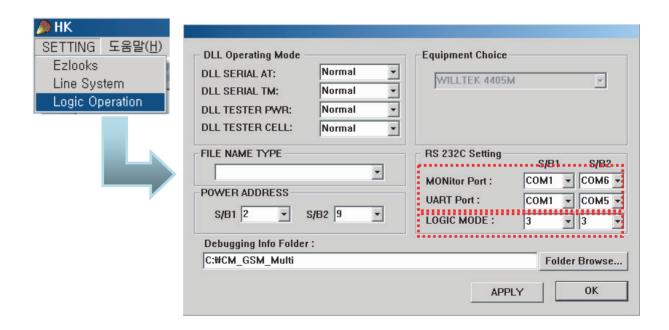
LED Number	Name	Description
LED 1	POWER	Power is provided for Test Jig
LED 2	TA	Indicate charging state of the phone battery
LED 3	UART	Indicate data transfer state through the UART port
LED 4	MON	Indicate data transfer state through the MON port

Table 12-3-3 LED Description

- 1. Connect as Fig 12-2(RS232 serial cable is connected between COM port of PC and MON port of TEST JIG, in general)
- 2. Set the Power Supply 4.0V
- 3. Set the 3rd, 4th of DIP SW ON state always
- 4. Press the Phone power key, if the Remote ON is used, 1st ON state

12.4 Procedure

- 1. Copy the file to C:\Cm Gsm Multi
- 2. Copy the files of((Windows XXX)MFCD DLL, vsflex7l_ocx_regist to C:\Cm_Gsm_Multi\dll,ocx
- 3. Select MFCD DLL of your computer OS
- 4. Click on "vsflex7l_ocx_regist"
- 5. Click on "Multi HK reg"
- 6. Connect as Fig 12-2 (RS232 serial cable is connected between COM port of PC, in general.)
- 7. Run HK 30exe to start calibration.
- 8. Click "Logic Operation" of "SETTING" menu bar



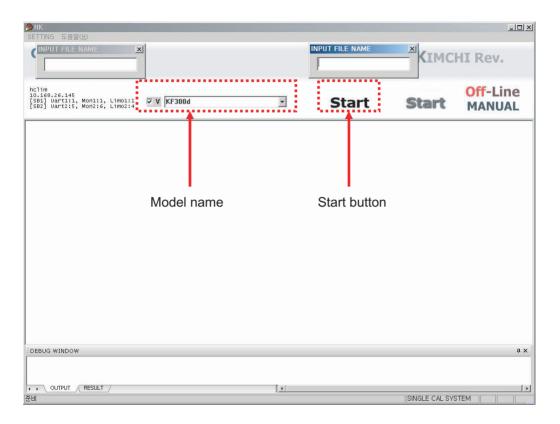
- 9. Set PORT (using RS232 cable) that PC can communicate with the phone
- 10. Select "LOGIC MODE" that you want

Logic mode: 1-> Calibration only

2-> Auto test only

3-> Cal & Auto

11. Select the model name "KF300d/KF300/KF300c"



12. Click "start" button

12.5 AGC

This procedure is for Rx calibration.

In this procedure, We can get RSSI correction value. Set band EGSM and press Start button the result window will show correction values per every power level and gain code and the same measure is performed per every frequency.

12.6 APC

This procedure is for Tx calibration.

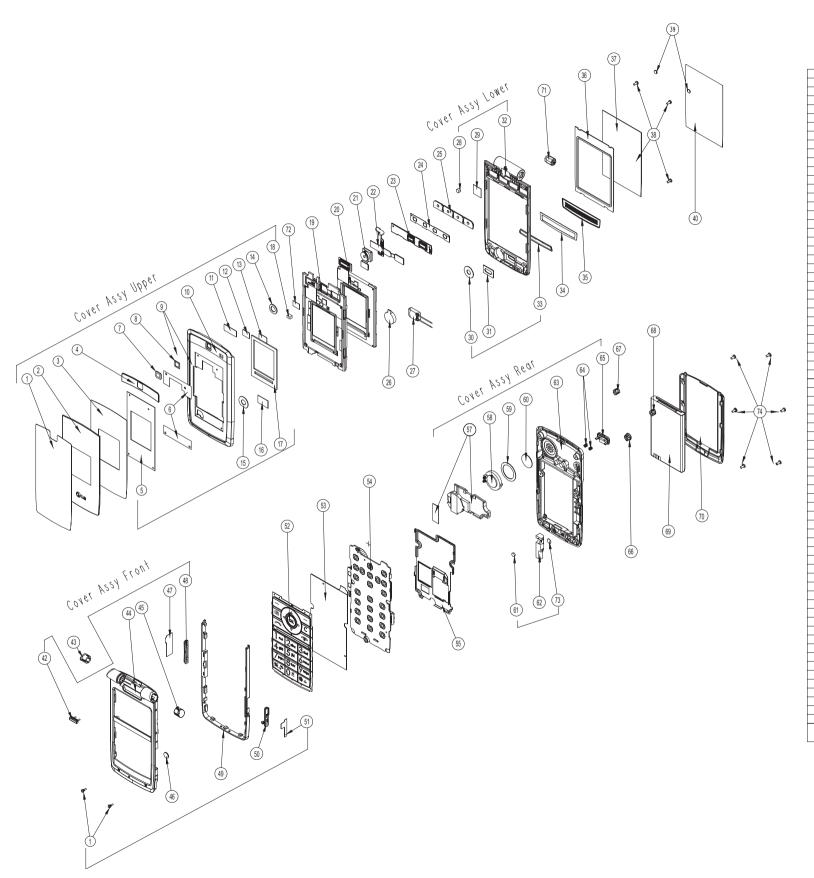
In this procedure you can get proper scale factor value and measured power level.

12.7 ADC

This procedure is for battery calibration.

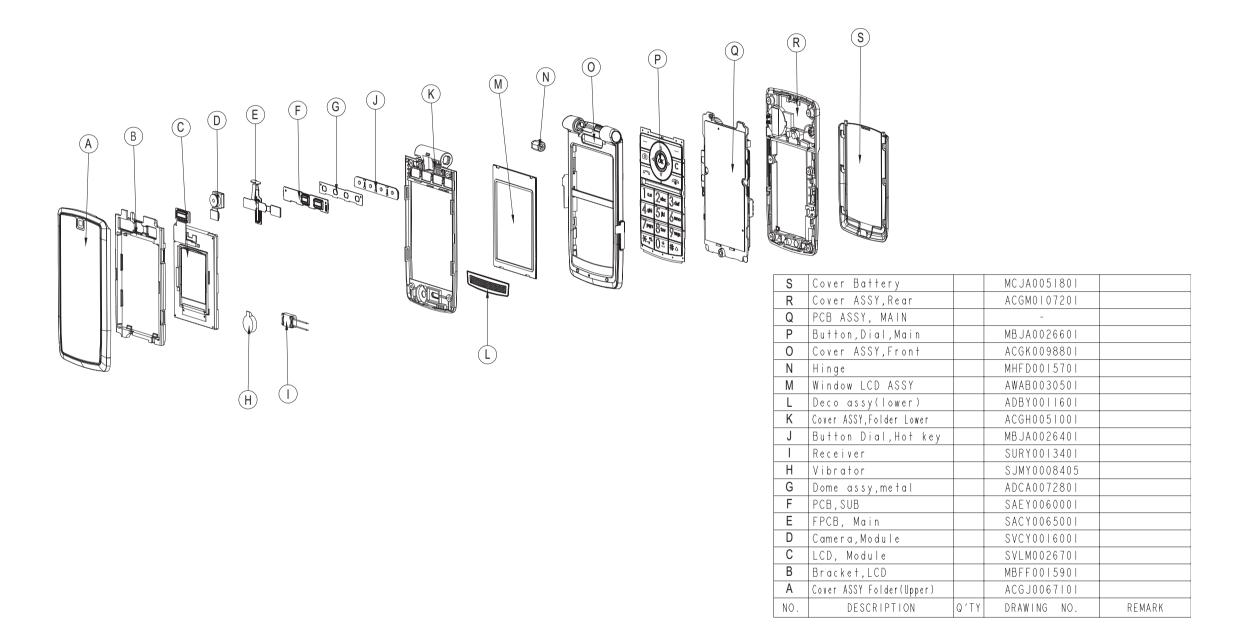
You can get main Battery Config Table and temperature Config Table will be reset.

13.1 EXPLODED VIEW



74	SCREW		GMEY0011201	
73	Label, A/S	6	MLAB0001102	
72	Tape Camera Folder	T i	MTAK0009601	
71	Hinge		MHFD0015701	
70	Cover Battery		MCJA005180#	
69	Battery	1	SBPL0092901	
68	Cap, screw,R		MCCH011530# MCCH011540#	
67	Cap, screw,L Cap,Mobile Switch	++-		
66 65	Locker,Battery	+ +	MCCF004780# MLEA004190#	
64	Spring, Coil	2	MSDZ0004190#	
63	Cover, Rear	1	MCJN007480#	
62	Anttena(BT)	i	SNGF0031202	
61	Pad, Mic		MPBH0034201	
60	Filter, speaker		MFBC0035201	
59	Pad, speaker		MPBN0048501	
58	Speaker		SUSY0025801	
57	Intenna	1	SNGF0033401(KF300,KF300e,KF300c)	SNGF0031101(KF300d)
56	PAD, Connector		MPBU0013901	
55 54	Shield Can	+ +	MCBA0024301 SAFY0245001	
53	PCB ASSY, MAIN Dome ASSY Metal	+ +	ADCA0073101	
52	Button, Dial, Main	+ +	MBJA002660#	Open:MBJA0029801,CIS:MBJA0029601 CHINA:MBJA0030201
51	Tape, Protection, MMI	- i i	MTAB0197901	CHINA:MBJA0030201
50	Cap, Recepticle	T i	MCCE0040901	
49	Deco, front	T i	MDAG0031401	
48	Button, side	1	MBJL0047101	
47	Tape, Protection, Volume		MTAB0197801	
46	Pad, MIC		MPBH0033801	
45	Deco, side_R		MDAC002120#	
44	Cover, Front		MCJK007920#	
43	Deco, side_L	+ +	MDAC002130#	
42	Stopper, Hinge Stopper, Folder	2	MSGB002290# MSGC000180#	
40	Tape, Protection	1	MTAB0206001	
39	Cap, Screw	2	MCCH012840#	
38	SCREW	4	GMEY0011201	
37	Window LCD((MAIN)		MWAC008740#	BK:1,PINK:2, WR&PP:3
36	Tape, window		MTAD0076601	
35	Deco, Folder Lower		MDAF000980#	BK:1,PINK:2, WR&PP:3
34	Tape, Deco(Folder, Lower		MTAA0 4890	
33	Filter, Receiver		MFBB0024301	
32	Cover, Folder Lower Pad, Receiver, lower	+ +	MCJH004100#	
31 30	Pad, Keceiver, lower	++-	MPBM0020401 MPBJ0048401	
29	PAD, Motor, lower Tape, Camera	+ +	MTAK0004201	
28	Magnet	- - 	MMAA000601	
27	Receiver	 	SURY0013401	
26	Vibrator	i	SJMY0008405	
25	Button Dial, Hot key	T i	MBJA002640#	
24	Dome assy, metal	i	ADCA0072801	
23	PCB,SUB	i	SAEY0060001	
22	FPCB, Main	1	SACY0065001	
21	Camera, Module		SVCY0016001	
20	LCD, Module		SVLM0026701	
19	Bracket, LCD	++-	MBFF0015901	
18 17	Gasket,Shield Form Pad, LCD(SUB)	+ +	MGAD0157901 MPBQ0033701	
16		++-	MPBM0020301	
15	PAD, Receiver PAD, Motor	++	MPBJ0048301	
14	Pad, Camera	- i i	MPBT0049401	
13	Pad, Connector(main)	T i	MPBU0013501	
12	Pad, Connector(camera)	i	MPBU0013301	
11	Pad, Connector(Icd)		MPBU0013401	
10	Cover Folder Upper		MCJJ005020#	
9	Tape, Deco(upper) Tape, Window(camera)		MTAA0 4860	
8	lape, Window(camera)		MTAD0076501	
7	Window, Camera	++-	MWAE0029401	
6	Tape, SUS	+ +	MTAZ0198001	
5 4	Plate	+++	MPFZ0030901 MDAE0041401	
3	Deco, Folder Upper Tape, Window(sub)	++-	MTAE0032801	
2	Window, LCD(sub)	+ +	MWAF003900#	
1	Tape, Protection	T i	MTAB0197701	
NO.	DESCRIPTION	Q'TY	DRAWING NO.	REMARK

ASS'Y EXPLODED VIEW



13.2 Replacement Parts Mechanic component>

Note: This Chapter is used for reference, Part order is ordered by SBOM standard on GCSC

Level	Location No.	Description	Part number	Spec		Remark
1		GSM(FOLDER)	TGFF0099601		Black	
4	MCJZ00	COVER	MCJZ0030501	1146*996*105_TDR_Reliance	Without Color	
4	MPCY00	PALLET	MPCY0013701	COMPLEX, (empty), , , , ,	Without Color	
4	MSCY00	SLEEVE	MSCY0001001	Deadspace Keeping Off_TDR_RLC	Without Color	
2	APEY00	PHONE	APEY0494001		Black	
3	ACGG00	COVER ASSY,FOLDER	ACGG0086101		Without Color	
4	ACGH00	COVER ASSY,FOLDER(LOWER)	ACGH0051001		Without Color	К
5	MCJH00	COVER,FOLDER(LOWER)	MCJH0041001	MOLD, PC LUPOY SC-1004A, , , , ,	Black	32
5	MFBB01	FILTER,RECEIVER	MFBB0024301	COMPLEX, (empty), , , , ,	Without Color	33
5	MMAA00	MAGNET,SWITCH	MMAA0000601	LG-G510,511,512 common use, DIA : 3.0mm+1.5t	Silver	28
5	MPBJ00	PAD,MOTOR	MPBJ0048401	COMPLEX, (empty), , , , ,	Without Color	30
5	МРВМ00	PAD,RECEIVER	MPBM0020401	COMPLEX, (empty), , , , ,	Without Color	31
5	MTAK00	TAPE,CAMERA	MTAK0004201	COMPLEX, (empty), , , , ,	Without Color	29
4	ACGJ00	COVER ASSY,FOLDER(UPPER)	ACGJ0067101		Without Color	А
5	MCJJ00	COVER,FOLDER(UPPER)	MCJJ0050201	MOLD, PC LUPOY SC-1004A, , , , ,	Black	10
5	MDAE00	DECO,FOLDER(UPPER)	MDAE0041401	PRESS, STS, , , , ,	Without Color	4
5	MGAD00	GASKET,SHIELD FORM	MGAD0157901	COMPLEX, (empty), , , , ,	Without Color	18
5	MICC00	INSERT,FRONT(UPPER)	MICC0010201	CUTTING, BeCu, , , , ,	Black	
5	MPBJ00	PAD,MOTOR	MPBJ0048301	COMPLEX, (empty), , , , ,	Without Color	15
5	МРВМ00	PAD,RECEIVER	MPBM0020301	COMPLEX, (empty), , , , ,	Without Color	16
5	MPBQ00	PAD,LCD(SUB)	MPBQ0033701	COMPLEX, (empty), , , , ,	Without Color	17
5	MPBT00	PAD,CAMERA	MPBT0049401	COMPLEX, (empty), , , , ,	Without Color	14
5	MPBU00	PAD,CONNECTOR	MPBU0013301	COMPLEX, (empty), , , , ,	Without Color	12
5	MPBU01	PAD,CONNECTOR	MPBU0013401	COMPLEX, (empty), , , , ,	Without Color	11
5	MPBU02	PAD,CONNECTOR	MPBU0013501	COMPLEX, (empty), , , , ,	Without Color	13
5	MPBZ00	PAD	MPBZ0202001	COMPLEX, (empty), , , , ,	Without Color	
5	MPFZ00	PLATE	MPFZ0030901	PRESS, STS, , , , ,	Without Color	5
5	MTAA00	TAPE,DECO	MTAA0148601	COMPLEX, (empty), , , , ,	Without Color	9
5	MTAB00	TAPE,PROTECTION	MTAB0197701	COMPLEX, (empty), , , , ,	Without Color	1
5	MTAD00	TAPE,WINDOW	MTAD0076501	COMPLEX, (empty), , , , ,	Without Color	8
5	MTAE00	TAPE,WINDOW(SUB)	MTAE0032801	COMPLEX, (empty), , , , ,	Without Color	3
5	MTAZ00	TAPE	MTAZ0198001	COMPLEX, (empty), , , , ,	Without Color	6

Level	Location No.	Description	Part number	Spec		Remark
5	MWAE00	WINDOW,CAMERA	MWAE0029401	COMPLEX, (empty), , , , ,	Without Color	7
5	MWAF00	WINDOW,LCD(SUB)	MWAF0039001	COMPLEX, (empty), , , , ,	Without Color	2
4	ACGK00	COVER ASSY,FRONT	ACGK0098801		Without Color	0
5	MBJL00	BUTTON,SIDE	MBJL0047101	COMPLEX, (empty), , , , ,	Without Color	48
5	MCCE00	CAP,RECEPTACLE	MCCE0040901	COMPLEX, (empty), , , , ,	Without Color	50
5	MCJK00	COVER,FRONT	MCJK0079201	MOLD, PC LUPOY SC-1004A, , , , ,	Black	44
5	MDAC01	DECO,SIDE	MDAC0021301	MOLD, PC LUPOY SC-1004A, , , , ,	Without Color	43
5	MDAG00	DECO,FRONT	MDAG0031401	MOLD, PC LUPOY SC-1004A, , , , ,	Without Color	49
5	MICC00	INSERT,FRONT(UPPER)	MICC0008901		Silver	
5	МРВН00	PAD,MIKE	MPBH0033801	COMPLEX, (empty), , , , ,	Without Color	46
5	MSGB00	STOPPER,HINGE	MSGB0022901	MOLD, Urethane Rubber S190A, , , , ,	Without Color	42
5	MSGC00	STOPPER,FOLDER	MSGC0001801	MOLD, Urethane Rubber S190A, , , , ,	Without Color	41
5	MTAB00	TAPE,PROTECTION	MTAB0197801	COMPLEX, (empty), , , , ,	Without Color	47
5	MTAB01	TAPE,PROTECTION	MTAB0197901	COMPLEX, (empty), , , , ,	Without Color	51
4	ADBY00	DECO ASSY	ADBY0011601	LOWER	Without Color	L
5	MDAF00	DECO,FOLDER(LOWER)	MDAF0009801	PRESS, STS, , , , ,	Black	35
5	MTAA00	TAPE,DECO	MTAA0148901	COMPLEX, (empty), , , , ,	Without Color	34
4	AWAB00	WINDOW ASSY,LCD	AWAB0030501		Without Color	М
5	MTAD00	TAPE,WINDOW	MTAD0076601	COMPLEX, (empty), , , , ,	Without Color	36
5	MWAC00	WINDOW,LCD	MWAC0087401	COMPLEX, (empty), , , , ,	Without Color	37
4	GMEY00	SCREW MACHINE,BIND	GMEY0011201	1.4 mm,3 mm,MSWR3(BK) ,N ,+ ,NYLOK	Without Color	74
4	MBFF00	BRACKET,LCD	MBFF0015901	CASTING, Mg Alloy, , , , ,	Without Color	19,B
4	MBJA00	BUTTON,DIAL	MBJA0026401	COMPLEX, (empty), , , , ,	Black	25,J
4	MBJA01	BUTTON,DIAL	MBJA0026601	COMPLEX, (empty), , , , ,	Black	52,P
4	MCCH01	CAP,SCREW	MCCH0128401	COMPLEX, (empty), , , , ,	Black	39
4	MDAC00	DECO,SIDE	MDAC0021201	MOLD, PC LUPOY SC-1004A, , , , ,	Without Color	45
4	MHFD00	HINGE,FOLDER	MHFD0015701	CASTING, STS, , , , ,	Without Color	71,N
4	MTAB00	TAPE,PROTECTION	MTAB0206001	COMPLEX, (empty), , , , ,	Without Color	40
4	MTAK00	TAPE,CAMERA	MTAK0009601	COMPLEX, (empty), , , , ,	Without Color	72
4	MFBC00	FILTER,SPEAKER	MFBC0035201	COMPLEX, (empty), , , , ,	Without Color	60
4	MLAB00	LABEL,A/S	MLAB0001102	C2000 USASV DIA 4.0	White	73
4	MLEA00	LOCKER,BATTERY	MLEA0041901	MOLD, PC LUPOY SC-1004A, , , , ,	Black	65
4	MPBH00	PAD,MIKE	MPBH0034201	COMPLEX, (empty), , , , ,	Without Color	61
4	MPBN00	PAD,SPEAKER	MPBN0048501	COMPLEX, (empty), , , , ,	Without Color	59

<Main component>

Note: This Chapter is used for reference, Part order is ordered by SBOM standard on GCSC

Level	Location No.	Description	Part number	Spec		Remark
4	SACY00	PCB ASSY,FLEXIBLE	SACY0065001	KF300_MAIN_FPCB		22,E
5	SACE00	PCB ASSY,FLEXIBLE,SMT	SACE0059301	KF300_MAIN_FPCB		
6	SACD00	PCB ASSY,FLEXIBLE,SMT TOP	SACD0049001			
7	CN801	CONNECTOR,BOARD TO BOARD	ENBY0023801	30 PIN,.4 mm,ETC , ,H=0.9, Header		
7	CN802	CONNECTOR,BOARD TO BOARD	ENBY0023201	44 PIN,0.4 mm,ETC , ,H=0.9, Header		
7	CN803	CONNECTOR,BOARD TO BOARD	ENBY0020202	60 PIN,0.4 mm,STRAIGHT ,AU ,STACKING HEIGHT 0.9 / HEADDER FOR KEYPAD TO MAIN		
6	SPCY	PCB,FLEXIBLE	SPCY0129001	FR-4 , mm,MULTI-6 , ,; , , , , , , ,		
4	SAEY00	PCB ASSY,KEYPAD	SAEY0060001			23,F
5	SAEB00	PCB ASSY,KEYPAD,INSERT	SAEB0022201			
6	ADCA00	DOME ASSY,METAL	ADCA0072801	FOLDER	Without Color	24,G
5	SAEE00	PCB ASSY,KEYPAD,SMT	SAEE0027001			
6	SAEC00	PCB ASSY,KEYPAD,SMT BOTTOM	SAEC0025401			
7	CN701	CONNECTOR,BOARD TO BOARD	ENBY0023901	30 PIN,0.4 mm,ETC , ,H=0.9, Socket		
7	CN702	CONNECTOR,BOARD TO BOARD	ENBY0020401	24 PIN,0.4 mm,ETC , ,H=0.9, Socket		
7	R701	RES,CHIP,MAKER	ERHZ0000505	680 ohm,1/16W ,J ,1005 ,R/TP		
7	R702	RES,CHIP,MAKER	ERHZ0000505	680 ohm,1/16W ,J ,1005 ,R/TP		
7	VA701	VARISTOR	SEVY0003801	18 V, ,SMD ,		
7	VA702	VARISTOR	SEVY0003801	18 V, ,SMD ,		
6	SPEY	PCB,KEYPAD	SPEY0054801	FR-4 ,0.5 mm,BUILD-UP 4 , ,; , , , , , , ,		
4	SJMY00	VIBRATOR,MOTOR	SJMY0008405	3 V,.08 A,10pi*2.7t ,12mm ,; ,3V , , ,12000rpm , , , ,310hm		26,H
4	SURY00	RECEIVER	SURY0013401	ASSY ,107 dB,32 ohm,11*07 , ,; , , , , , , , CONNECTOR ,		27,I
4	SVCY00	CAMERA	SVCY0016001	CMOS ,MEGA ,2M FF Toshiba 1/4" Sensor		21,D
4	SVLM00	LCD MODULE	SVLM0026701	MAIN ,M_240*320 S_128*160 ,41*57.5*3.3 ,262k ,TFT ,TM ,M_LGDP4531 S_LGDP4512 ,		20,C
3	ACGM00	COVER ASSY,REAR	ACGM0099701		Without Color	
4	MCCF00	CAP,MOBILE SWITCH	MCCF0047801	COMPLEX, (empty), , , , ,	Black	66
4	MCJN00	COVER,REAR	MCJN0074801	MOLD, PC LUPOY SC-1004A, , , , ,	Black	63
4	MSDB00	SPRING,COIL	MSDB0004501	COMPLEX, (empty), , , , ,	Silver	
4	SNGF00	ANTENNA,GSM,FIXED	SNGF0031101	3.0 ,-2.0 dBd,, ,internal, GSM850/1800/1900 ,; ,TRIPLE ,- 2.0 ,50 ,3.0		57

Level	Location No.	Description	Part number	Spec		Remark
4	SNGF01	ANTENNA,GSM,FIXED	SNGF0031202	3.0 ,-2.0 dBd,, ,internal, bluetooth ,; ,SINGLE ,-2.0 ,50 ,3.0		62
4	SUSY00	SPEAKER	SUSY0025801	PIN ,8 ohm,89 dB,16 mm, ,; , , , , , , , , CONTACT		58
3	GMEY00	SCREW MACHINE,BIND	GMEY0011201	1.4 mm,3 mm,MSWR3(BK) ,N ,+ ,NYLOK	Without Color	38
3	мссноо	CAP,SCREW	MCCH0115301	COMPLEX, (empty), , , , ,	Black	68
3	MCCH01	CAP,SCREW	MCCH0115401	COMPLEX, (empty), , , , ,	Black	67
3	MLAK00	LABEL,MODEL	MLAK0010802	PRINTING, (empty), , , , ,	Without Color	
3	SAFY00	PCB ASSY,MAIN	SAFY0245001			54
4	SAFB00	PCB ASSY,MAIN,INSERT	SAFB0080301			
5	ADCA00	DOME ASSY,METAL	ADCA0073101	LOWER	Without Color	53
5	MCBA00	CAN,SHIELD	MCBA0024301	COMPLEX, (empty), , , , ,	Without Color	55
5	MGAD00	GASKET,SHIELD FORM	MGAD0158101	COMPLEX, (empty), , , , ,	Without Color	
5	SPKY00	PCB,SIDEKEY	SPKY0056601	FR-4 , mm,DOUBLE , ,; , , , , , , ,		
5	SUMY00	MICROPHONE	SUMY0010301	FPCB ,-42 dB,4*1.5T ,Standard Holder		
4	SAFF00	PCB ASSY,MAIN,SMT	SAFF0162201			
5	MLAZ00	LABEL	MLAZ0038301	PID Label 4 Array	Without Color	
5	SAFC00	PCB ASSY,MAIN,SMT BOTTOM	SAFC0103201			
6	BAT100	BATTERY,CELL,LITHIUM	SBCL0001701	2 V,0.5 mAh,CYLINDER ,Reflow type BB, Max T 1.67, phi 4.8, Pb-Free		
6	C100	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP		
6	C101	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C102	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C103	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP		
6	C104	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP		
6	C105	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C106	CAP,CHIP,MAKER	ECZH0025502	22000000 pF,6.3V ,M ,X5R ,HD ,2012 ,R/TP ,; ,0.85t ,[empty] ,[empty] ,[empty] ,[empty] ,[empty] ,[empty]		
6	C107	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C108	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP		
6	C109	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C110	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C111	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP		
6	C112	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP		
6	C113	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP		
6	C114	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP		
6	C115	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP		
6	C116	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP		
6	C117	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP		

Level	Location No.	Description	Part number	Spec	Remark
6	C118	CAP,CHIP,MAKER	ECZH0025502	22000000 pF,6.3V ,M ,X5R ,HD ,2012 ,R/TP ,; ,0.85t ,[empty] ,[empty] ,[empty] ,[empty] ,[empty]	
6	C119	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	
6	C120	CAP,CERAMIC,CHIP	ECCH0000143	1 nF,50V,K,X7R,HD,1005,R/TP	
6	C121	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	C122	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	C123	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	C124	CAP,CHIP,MAKER	ECZH0025502	22000000 pF,6.3V ,M ,X5R ,HD ,2012 ,R/TP ,; ,0.85t ,[empty] ,[empty] ,[empty] ,[empty] ,[empty]	
6	C125	CAP,CHIP,MAKER	ECZH0025502	22000000 pF,6.3V ,M ,X5R ,HD ,2012 ,R/TP ,; ,0.85t ,[empty] ,[empty] ,[empty] ,[empty] ,[empty]	
6	C126	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	C127	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	C128	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	C129	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	C130	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	C131	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	C132	CAP,CERAMIC,CHIP	ECCH0000198	2.2 uF,6.3V ,M ,X5R ,TC ,1005 ,R/TP	
6	C133	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	C134	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	C135	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	
6	C136	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	C137	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	C138	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP	
6	C139	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP	
6	C140	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	
6	C141	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	
6	C142	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP	
6	C143	CAP,CERAMIC,CHIP	ECCH0000120	39 pF,50V,J,NP0,TC,1005,R/TP	
6	C144	CAP,CERAMIC,CHIP	ECCH0000120	39 pF,50V,J,NP0,TC,1005,R/TP	
6	C145	CAP,CERAMIC,CHIP	ECCH0000120	39 pF,50V,J,NP0,TC,1005,R/TP	
6	C146	CAP,CERAMIC,CHIP	ECCH0000120	39 pF,50V,J,NP0,TC,1005,R/TP	
6	C149	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP	
6	C150	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP	
6	C151	CAP,CERAMIC,CHIP	ECCH0000120	39 pF,50V,J,NP0,TC,1005,R/TP	
6	C152	CAP,CERAMIC,CHIP	ECCH0000120	39 pF,50V,J,NP0,TC,1005,R/TP	
6	C153	CAP,CERAMIC,CHIP	ECCH0000120	39 pF,50V,J,NP0,TC,1005,R/TP	
6	C154	CAP,CERAMIC,CHIP	ECCH0000120	39 pF,50V,J,NP0,TC,1005,R/TP	

Level	Location No.	Description	Part number	Spec	Remark
6	C157	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP	
6	C158	CAP,CHIP,MAKER	ECZH0000813	100 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	
6	C202	CAP,CERAMIC,CHIP	ECCH0000143	1 nF,50V,K,X7R,HD,1005,R/TP	
6	C203	CAP,CERAMIC,CHIP	ECCH0000143	1 nF,50V,K,X7R,HD,1005,R/TP	
6	C204	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP	
6	C205	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP	
6	C207	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP	
6	C209	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP	
6	C210	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	C211	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	C212	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	C215	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	C217	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	C300	CAP,CERAMIC,CHIP	ECCH0005604	10 uF,6.3V ,M ,X5R ,TC ,1608 ,R/TP	
6	C301	CAP,CERAMIC,CHIP	ECCH0000120	39 pF,50V,J,NP0,TC,1005,R/TP	
6	C302	CAP,TANTAL,CHIP	ECTH0005202	100 uF,4V ,M ,L_ESR ,2012 ,R/TP ,; , ,[empty] ,[empty] , ,[empty] , ,[empty] ,[empty] ,[empty] ,	
6	C303	CAP,TANTAL,CHIP	ECTH0005202	100 uF,4V ,M ,L_ESR ,2012 ,R/TP ,; , ,[empty] ,[empty] , ,[empty] , ,[empty] ,[empty] ,[empty] ,	
6	C304	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	C305	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP	
6	C306	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP	
6	C307	CAP,CERAMIC,CHIP	ECCH0005604	10 uF,6.3V ,M ,X5R ,TC ,1608 ,R/TP	
6	C308	CAP,CHIP,MAKER	ECZH0003503	1 uF,25V ,K ,X5R ,HD ,1608 ,R/TP	
6	C309	CAP,CERAMIC,CHIP	ECCH0000122	47 pF,50V,J,NP0,TC,1005,R/TP	
6	C310	CAP,CHIP,MAKER	ECZH0003503	1 uF,25V ,K ,X5R ,HD ,1608 ,R/TP	
6	C311	CAP,CERAMIC,CHIP	ECCH0000122	47 pF,50V,J,NP0,TC,1005,R/TP	
6	C312	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	C313	CAP,CERAMIC,CHIP	ECCH0000122	47 pF,50V,J,NP0,TC,1005,R/TP	
6	C314	CAP,CERAMIC,CHIP	ECCH0000104	3 pF,50V,C,NP0,TC,1005,R/TP	
6	C315	CAP,CERAMIC,CHIP	ECCH0005604	10 uF,6.3V ,M ,X5R ,TC ,1608 ,R/TP	
6	C316	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	
6	C317	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	
6	C318	CAP,CHIP,MAKER	ECZH0001216	220 nF,10V ,K ,X5R ,TC ,1005 ,R/TP	
6	C319	CAP,CERAMIC,CHIP	ECCH0005604	10 uF,6.3V ,M ,X5R ,TC ,1608 ,R/TP	
6	C321	CAP,CERAMIC,CHIP	ECCH0000143	1 nF,50V,K,X7R,HD,1005,R/TP	
6	C322	CAP,CERAMIC,CHIP	ECCH0000143	1 nF,50V,K,X7R,HD,1005,R/TP	
6	C324	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	

Level	Location No.	Description	Part number	Spec	Remark
6	C325	CAP,CERAMIC,CHIP	ECCH0000143	1 nF,50V,K,X7R,HD,1005,R/TP	
6	C326	CAP,CERAMIC,CHIP	ECCH0000120	39 pF,50V,J,NP0,TC,1005,R/TP	
6	C327	CAP,CERAMIC,CHIP	ECCH0005604	10 uF,6.3V ,M ,X5R ,TC ,1608 ,R/TP	
6	C328	CAP,CERAMIC,CHIP	ECCH0000120	39 pF,50V,J,NP0,TC,1005,R/TP	
6	C329	CAP,CERAMIC,CHIP	ECCH0000198	2.2 uF,6.3V ,M ,X5R ,TC ,1005 ,R/TP	
6	C330	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	C331	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	C501	CAP,CERAMIC,CHIP	ECCH0000120	39 pF,50V,J,NP0,TC,1005,R/TP	
6	C502	CAP,CERAMIC,CHIP	ECCH0000120	39 pF,50V,J,NP0,TC,1005,R/TP	
6	C503	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP	
6	C504	CAP,CHIP,MAKER	ECZH0000841	56 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	
6	C505	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	C506	CAP,CERAMIC,CHIP	ECCH0000198	2.2 uF,6.3V ,M ,X5R ,TC ,1005 ,R/TP	
6	C507	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	C508	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP	
6	C509	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP	
6	C510	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP	
6	C511	CAP,CERAMIC,CHIP	ECCH0000117	27 pF,50V,J,NP0,TC,1005,R/TP	
6	C517	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	C518	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	C519	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	C520	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	C523	CAP,CERAMIC,CHIP	ECCH0000198	2.2 uF,6.3V ,M ,X5R ,TC ,1005 ,R/TP	
6	C601	CAP,CHIP,MAKER	ECZH0025502	22000000 pF,6.3V ,M ,X5R ,HD ,2012 ,R/TP ,; ,0.85t ,[empty] ,[empty] ,[empty] ,[empty] ,[empty] ,[empty]	
6	C602	CAP,CHIP,MAKER	ECZH0000830	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	
6	C603	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	
6	C604	CAP,CERAMIC,CHIP	ECCH0000120	39 pF,50V,J,NP0,TC,1005,R/TP	
6	C605	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	
6	C606	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	
6	C608	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	
6	C609	CAP,CHIP,MAKER	ECZH0001002	0.5 pF,50V ,B ,NP0 ,TC ,1005 ,R/TP	
6	C611	CAP,CHIP,MAKER	ECZH0000830	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	
6	C612	INDUCTOR,CHIP	ELCH0004733	4.3 nH,S ,1005 ,R/TP ,Coil	
6	C613	CAP,CERAMIC,CHIP	ECCH0000117	27 pF,50V,J,NP0,TC,1005,R/TP	
6	C614	CAP,CERAMIC,CHIP	ECCH0000117	27 pF,50V,J,NP0,TC,1005,R/TP	
6	C616	CAP,CERAMIC,CHIP	ECCH0000175	2.7 pF,50V ,B ,NP0 ,TC ,1005 ,R/TP	

Level	Location No.	Description	Part number	Spec	Remark
6	C617	CAP,CERAMIC,CHIP	ECCH0000127	82 pF,50V,J,NP0,TC,1005,R/TP	
6	C618	CAP,CERAMIC,CHIP	ECCH0000122	47 pF,50V,J,NP0,TC,1005,R/TP	
6	C619	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	C620	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP	
6	C621	CAP,CERAMIC,CHIP	ECCH0000107	6 pF,50V,D,NP0,TC,1005,R/TP	
6	C622	CAP,CHIP,MAKER	ECZH0001216	220 nF,10V ,K ,X5R ,TC ,1005 ,R/TP	
6	C623	CAP,CERAMIC,CHIP	ECCH0000107	6 pF,50V,D,NP0,TC,1005,R/TP	
6	C624	CAP,CHIP,MAKER	ECZH0000839	4.7 pF,50V ,C ,NP0 ,TC ,1005 ,R/TP	
6	C625	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP	
6	C626	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP	
6	C627	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP	
6	C628	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP	
6	C629	CAP,CERAMIC,CHIP	ECCH0000117	27 pF,50V,J,NP0,TC,1005,R/TP	
6	C630	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP	
6	C631	CAP,CHIP,MAKER	ECZH0000839	4.7 pF,50V ,C ,NP0 ,TC ,1005 ,R/TP	
6	C632	CAP,CERAMIC,CHIP	ECCH0000120	39 pF,50V,J,NP0,TC,1005,R/TP	
6	C633	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP	
6	C634	CAP,CHIP,MAKER	ECZH0003103	0.1 uF,10V ,K ,X7R ,HD ,1005 ,R/TP	
6	C635	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP	
6	C636	CAP,CERAMIC,CHIP	ECCH0000120	39 pF,50V,J,NP0,TC,1005,R/TP	
6	C637	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP	
6	C638	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP	
6	C639	CAP,CHIP,MAKER	ECZH0000813	100 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	
6	C640	CAP,CHIP,MAKER	ECZH0000813	100 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	
6	C641	CAP,CHIP,MAKER	ECZH0000813	100 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	
6	C642	CAP,CERAMIC,CHIP	ECCH0000127	82 pF,50V,J,NP0,TC,1005,R/TP	
6	C643	CAP,CHIP,MAKER	ECZH0000813	100 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	
6	C644	CAP,CHIP,MAKER	ECZH0000813	100 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	
6	CN300	CONNECTOR,I/O	ENRY0006801	18 PIN,0.4 mm,ETC , , ,; ,18 ,0.40MM ,ANGLE ,RECEPTACLE ,SMD ,R/TP ,	
6	CN301	CONNECTOR,ETC	ENZY0020401	3 PIN,2.5 mm,BOTTOM , ,	
6	CN500	CONNECTOR,BOARD TO BOARD	ENBY0020402	60 PIN,0.4 mm,STRAIGHT ,AU ,STACKING HEIGHT 0.9 / SOCKET FOR KEYPAD TO MAIN	
6	D100	DIODE,SWITCHING	EDSY0017301	VSM ,15 V,100 mA,R/TP ,PB-FREE	
6	D501	DIODE,TVS	EDTY0009401	VMN2 ,5 V,10 W,R/TP ,1.0*0.6*0.4 ,; , ,7.82V , , ,100mW ,[empty] ,[empty] ,2P ,1	
6	D502	DIODE,TVS	EDTY0009401	VMN2 ,5 V,10 W,R/TP ,1.0*0.6*0.4 ,; , ,7.82V , , ,100mW ,[empty] ,[empty] ,2P ,1	

Level	Location No.	Description	Part number	Spec	Remark
6	D503	DIODE,TVS	EDTY0009401	VMN2 ,5 V,10 W,R/TP ,1.0*0.6*0.4 ,; , ,7.82V , , ,100mW ,[empty] ,[empty] ,2P ,1	
6	D504	DIODE,TVS	EDTY0009401	VMN2 ,5 V,10 W,R/TP ,1.0*0.6*0.4 ,; , ,7.82V , , ,100mW ,[empty] ,[empty] ,2P ,1	
6	D505	DIODE,TVS	EDTY0009401	VMN2 ,5 V,10 W,R/TP ,1.0*0.6*0.4 ,; , ,7.82V , , ,100mW ,[empty] ,[empty] ,2P ,1	
6	D506	DIODE,TVS	EDTY0009401	VMN2 ,5 V,10 W,R/TP ,1.0*0.6*0.4 ,; , ,7.82V , , ,100mW ,[empty] ,[empty] ,2P ,1	
6	FB100	FILTER,BEAD,CHIP	SFBH0008101	600 ohm,1005 ,	
6	FB300	FILTER,BEAD,CHIP	SFBH0008105	1800 ohm,1005 ,Chip bead ,; ,1800ohm ,; ,[empty] ,R/TP	
6	FB301	FILTER,BEAD,CHIP	SFBH0008105	1800 ohm,1005 ,Chip bead ,; ,1800ohm ,; ,[empty] ,R/TP	
6	FB302	FILTER,BEAD,CHIP	SFBH0008105	1800 ohm,1005 ,Chip bead ,; ,1800ohm ,; ,[empty] ,R/TP	
6	FB304	FILTER,BEAD,CHIP	SFBH0007101	120 ohm,1005 ,Ferrite Bead	
6	FB305	FILTER,BEAD,CHIP	SFBH0007101	120 ohm,1005 ,Ferrite Bead	
6	FB500	FILTER,BEAD,CHIP	SFBH0008101	600 ohm,1005 ,	
6	FL500	FILTER,EMI/POWER	SFEY0011601	SMD ,SMD ,18 V,4ch. EMI_ESD Filter (50 Ohm,15pF)	
6	FL501	FILTER,EMI/POWER	SFEY0012501	SMD ,SMD ,18 V,4ch. EMI_ESD Filter (200 Ohm,25pF)	
6	FL502	FILTER,EMI/POWER	SFEY0011601	SMD ,SMD ,18 V,4ch. EMI_ESD Filter (50 Ohm,15pF)	
6	FL503	FILTER,EMI/POWER	SFEY0011601	SMD ,SMD ,18 V,4ch. EMI_ESD Filter (50 Ohm,15pF)	
6	FL504	FILTER,EMI/POWER	SFEY0012501	SMD ,SMD ,18 V,4ch. EMI_ESD Filter (200 Ohm,25pF)	
6	FL505	FILTER,EMI/POWER	SFEY0012501	SMD ,SMD ,18 V,4ch. EMI_ESD Filter (200 Ohm,25pF)	
6	FL506	FILTER,EMI/POWER	SFEY0011601	SMD ,SMD ,18 V,4ch. EMI_ESD Filter (50 Ohm,15pF)	
6	FL507	FILTER,EMI/POWER	SFEY0012501	SMD ,SMD ,18 V,4ch. EMI_ESD Filter (200 Ohm,25pF)	
6	FL508	FILTER,EMI/POWER	SFEY0010501	SMD ,SMD ,18 V,4ch. EMI_ESD Filter (100Ohm,15pF), Pb-free	
6	FL601	FILTER,SEPERATOR	SFAY0011101	850.900 ,1800.1900 ,3.8 dB,4.1 dB, dB, dB,4532 ,4.5X3.2 Size Quad Band FEM	
6	J300	CONN,SOCKET	ENSY0018701	6 PIN,ETC , ,2.54 mm,H=1.8	
6	J301	CONN,SOCKET	ENSY0017701	8 PIN,ETC , , mm,Micro-SD, Hinge type	
6	L100	INDUCTOR,SMD,POWER	ELCP0008001	4.7 uH,M ,2.5*2.0*1.0 ,R/TP ,	
6	L300	INDUCTOR,CHIP	ELCH0010402	270 nH,M ,1005 ,R/TP ,CHIP	
6	L301	INDUCTOR,CHIP	ELCH0003842	100 nH,J ,1005 ,R/TP ,MLCI	
6	L500	INDUCTOR,CHIP	ELCH0004714	18 nH,J ,1005 ,R/TP ,	
6	L501	INDUCTOR,CHIP	ELCH0004714	18 nH,J ,1005 ,R/TP ,	
6	L601	INDUCTOR,CHIP	ELCH0005013	4.7 nH,S ,1005 ,R/TP ,	
6	L602	INDUCTOR,CHIP	ELCH0005014	5.6 nH,S ,1005 ,R/TP ,	
6	L603	INDUCTOR,CHIP	ELCH0001052	18 nH,J ,1005 ,R/TP ,PBFREE	
6	L604	INDUCTOR,CHIP	ELCH0001052	18 nH,J ,1005 ,R/TP ,PBFREE	
6	Q400	TR,BJT,ARRAY	EQBA0004902	TES6 ,200 mW,R/TP ,NPN/PNP dual, Vo1=50V, lo1=100mA, Vo2=-50V,lo2=-100mA	

Level	Location No.	Description	Part number	Spec	Remark
6	R100	RES,CHIP,MAKER	ERHZ0000406	100 Kohm,1/16W ,J ,1005 ,R/TP	
6	R101	RES,CHIP,MAKER	ERHZ0000406	100 Kohm,1/16W ,J ,1005 ,R/TP	
6	R102	RES,CHIP,MAKER	ERHZ0000485	4700 ohm,1/16W ,J ,1005 ,R/TP	
6	R103	RES,CHIP	ERHY0000512	10M ohm,1/16W,J,1608,R/TP	
6	R105	RES,CHIP,MAKER	ERHZ0000405	10 Kohm,1/16W ,J ,1005 ,R/TP	
6	R106	RES,CHIP,MAKER	ERHZ0000312	68 Kohm,1/16W ,F ,1005 ,R/TP	
6	R107	RES,CHIP,MAKER	ERHZ0000486	47 Kohm,1/16W ,J ,1005 ,R/TP	
6	R109	RES,CHIP,MAKER	ERHZ0000405	10 Kohm,1/16W ,J ,1005 ,R/TP	
6	R110	RES,CHIP,MAKER	ERHZ0000405	10 Kohm,1/16W ,J ,1005 ,R/TP	
6	R120	RES,CHIP,MAKER	ERHZ0000213	120 Kohm,1/16W ,F ,1005 ,R/TP	
6	R204	RES,CHIP,MAKER	ERHZ0000406	100 Kohm,1/16W ,J ,1005 ,R/TP	
6	R205	RES,CHIP,MAKER	ERHZ0000406	100 Kohm,1/16W ,J ,1005 ,R/TP	
6	R206	RES,CHIP,MAKER	ERHZ0000486	47 Kohm,1/16W ,J ,1005 ,R/TP	
6	R207	RES,CHIP,MAKER	ERHZ0000486	47 Kohm,1/16W ,J ,1005 ,R/TP	
6	R210	RES,CHIP,MAKER	ERHZ0000405	10 Kohm,1/16W ,J ,1005 ,R/TP	
6	R211	RES,CHIP,MAKER	ERHZ0000460	30 Kohm,1/16W ,J ,1005 ,R/TP	
6	R212	RES,CHIP,MAKER	ERHZ0000406	100 Kohm,1/16W ,J ,1005 ,R/TP	
6	R213	RES,CHIP	ERHY0000140	36K ohm,1/16W,F,1005,R/TP	
6	R214	RES,CHIP,MAKER	ERHZ0000406	100 Kohm,1/16W ,J ,1005 ,R/TP	
6	R216	RES,CHIP,MAKER	ERHZ0000405	10 Kohm,1/16W ,J ,1005 ,R/TP	
6	R217	RES,CHIP,MAKER	ERHZ0000460	30 Kohm,1/16W ,J ,1005 ,R/TP	
6	R218	RES,CHIP,MAKER	ERHZ0000406	100 Kohm,1/16W ,J ,1005 ,R/TP	
6	R219	RES,CHIP,MAKER	ERHZ0000483	47 ohm,1/16W ,J ,1005 ,R/TP	
6	R300	RES,CHIP,MAKER	ERHZ0000529	1.5 Kohm,1/16W ,J ,1005 ,R/TP	
6	R302	RES,CHIP,MAKER	ERHZ0000443	2200 ohm,1/16W ,J ,1005 ,R/TP	
6	R303	RES,CHIP,MAKER	ERHZ0000407	1000 Kohm,1/16W ,J ,1005 ,R/TP	
6	R304	RES,CHIP,MAKER	ERHZ0000406	100 Kohm,1/16W ,J ,1005 ,R/TP	
6	R305	RES,CHIP,MAKER	ERHZ0000406	100 Kohm,1/16W ,J ,1005 ,R/TP	
6	R306	RES,CHIP,MAKER	ERHZ0000406	100 Kohm,1/16W ,J ,1005 ,R/TP	
6	R307	RES,CHIP,MAKER	ERHZ0000488	4.7 ohm,1/16W ,J ,1005 ,R/TP	
6	R308	RES,CHIP,MAKER	ERHZ0000406	100 Kohm,1/16W ,J ,1005 ,R/TP	
6	R309	RES,CHIP,MAKER	ERHZ0000488	4.7 ohm,1/16W ,J ,1005 ,R/TP	
6	R310	RES,CHIP,MAKER	ERHZ0000483	47 ohm,1/16W ,J ,1005 ,R/TP	
6	R311	RES,CHIP,MAKER	ERHZ0000483	47 ohm,1/16W ,J ,1005 ,R/TP	
6	R312	RES,CHIP,MAKER	ERHZ0000434	1 ohm,1/16W ,J ,1005 ,R/TP	
6	R314	RES,CHIP,MAKER	ERHZ0000486	47 Kohm,1/16W ,J ,1005 ,R/TP	
6	R315	RES,CHIP,MAKER	ERHZ0000486	47 Kohm,1/16W ,J ,1005 ,R/TP	

Level	Location No.	Description	Part number	Spec	Remark
6	R316	RES,CHIP,MAKER	ERHZ0000422	15 Kohm,1/16W ,J ,1005 ,R/TP	
6	R317	RES,CHIP,MAKER	ERHZ0000406	100 Kohm,1/16W ,J ,1005 ,R/TP	
6	R318	RES,CHIP,MAKER	ERHZ0000404	1 Kohm,1/16W ,J ,1005 ,R/TP	
6	R319	RES,CHIP,MAKER	ERHZ0000406	100 Kohm,1/16W ,J ,1005 ,R/TP	
6	R320	RES,CHIP,MAKER	ERHZ0000406	100 Kohm,1/16W ,J ,1005 ,R/TP	
6	R321	RES,CHIP,MAKER	ERHZ0000406	100 Kohm,1/16W ,J ,1005 ,R/TP	
6	R322	RES,CHIP,MAKER	ERHZ0000443	2200 ohm,1/16W ,J ,1005 ,R/TP	
6	R323	RES,CHIP,MAKER	ERHZ0000406	100 Kohm,1/16W ,J ,1005 ,R/TP	
6	R324	RES,CHIP	ERHY0003301	100 ohm,1/16W ,J ,1005 ,R/TP	
6	R326	RES,CHIP	ERHY0003301	100 ohm,1/16W ,J ,1005 ,R/TP	
6	R327	RES,CHIP,MAKER	ERHZ0000443	2200 ohm,1/16W ,J ,1005 ,R/TP	
6	R328	RES,CHIP,MAKER	ERHZ0000407	1000 Kohm,1/16W ,J ,1005 ,R/TP	
6	R329	RES,CHIP,MAKER	ERHZ0000406	100 Kohm,1/16W ,J ,1005 ,R/TP	
6	R400	RES,CHIP,MAKER	ERHZ0000483	47 ohm,1/16W ,J ,1005 ,R/TP	
6	R401	RES,CHIP,MAKER	ERHZ0000483	47 ohm,1/16W ,J ,1005 ,R/TP	
6	R402	RES,CHIP,MAKER	ERHZ0000505	680 ohm,1/16W ,J ,1005 ,R/TP	
6	R403	RES,CHIP,MAKER	ERHZ0000505	680 ohm,1/16W ,J ,1005 ,R/TP	
6	R404	RES,CHIP,MAKER	ERHZ0000505	680 ohm,1/16W ,J ,1005 ,R/TP	
6	R405	RES,CHIP,MAKER	ERHZ0000505	680 ohm,1/16W ,J ,1005 ,R/TP	
6	R406	RES,CHIP,MAKER	ERHZ0000405	10 Kohm,1/16W ,J ,1005 ,R/TP	
6	R408	RES,CHIP,MAKER	ERHZ0003701	2.2 ohm,1/16W ,J ,1608 ,R/TP	
6	R500	RES,CHIP,MAKER	ERHZ0000406	100 Kohm,1/16W ,J ,1005 ,R/TP	
6	R501	RES,CHIP,MAKER	ERHZ0000485	4700 ohm,1/16W ,J ,1005 ,R/TP	
6	R502	RES,CHIP,MAKER	ERHZ0000485	4700 ohm,1/16W ,J ,1005 ,R/TP	
6	R503	RES,CHIP,MAKER	ERHZ0000406	100 Kohm,1/16W ,J ,1005 ,R/TP	
6	R504	RES,CHIP	ERHY0003301	100 ohm,1/16W ,J ,1005 ,R/TP	
6	R603	RES,CHIP,MAKER	ERHZ0000404	1 Kohm,1/16W ,J ,1005 ,R/TP	
6	R607	RES,CHIP,MAKER	ERHZ0000490	51 ohm,1/16W ,J ,1005 ,R/TP	
6	R610	RES,CHIP,MAKER	ERHZ0000512	82 ohm,1/16W ,J ,1005 ,R/TP	
6	R611	RES,CHIP,MAKER	ERHZ0000405	10 Kohm,1/16W ,J ,1005 ,R/TP	
6	R612	RES,CHIP,MAKER	ERHZ0000402	10 ohm,1/16W ,J ,1005 ,R/TP	
6	R614	RES,CHIP,MAKER	ERHZ0000505	680 ohm,1/16W ,J ,1005 ,R/TP	
6	SW601	CONN,RF SWITCH	ENWY0004501	,SMD , dB,H=3.6, Straight type	
6	U100	IC	EUSY0313101	BGA ,144 PIN,R/TP ,EGPRS Quad band ABB Stratos-S	
6	U101	IC	EUSY0313501	BGA ,291 PIN,R/TP ,EGPRS Digital Base band, LEMANS	
6	U201	MODULE,ETC	SMZY0015001	6.3 * 5.3 * 1.3mm , 63 PIN, Bluetooth Module(BT+FM)	

Level	Location No.	Description	Part number	Spec	Remark
6	U202	IC	EUSY0286002	BGA ,105 PIN,R/TP ,512M 65nm Nor+128MSDRAM, 1.8V I/O,Pb Free , ,IC,MCP	
6	U203	IC	EUSY0254701	DFN 3*3*0.9 ,10 PIN,R/TP ,Charger IC, I Max 1A, Wall Adaptor/USB Charger	
6	U204	IC	EUSY0319201	DFN ,10 PIN,R/TP ,OVP	
6	U300	DIODE,TVS	EDTY0006501	SC70-6L ,5.25 V,100 W,R/TP ,	
6	U301	IC	EUSY0300101	WQFN ,10 PIN,R/TP ,Small package Dual SPDT analog Switch, PB-Free	
6	U302	IC	EUSY0317101	WQFN ,10 PIN,R/TP ,1.8*1.4*0.75	
6	U303	IC	EUSY0160001	MicroStar Junior ,15 PIN,R/TP ,1.1W Class-D Mono Audio AMP	
6	U304	IC	EUSY0299301	SON1612-6 ,6 PIN,R/TP ,2.5V 150mA LDO Pb-Free	
6	U500	IC	EUSY0319001	WDFN-8L ,8 PIN,R/TP ,300mA/300mA 2.8V/1.8V Dual LDO	
6	U501	IC	EUSY0336502	, PIN,R/TP , ,; ,IC,Charge Pump	
6	U601	PAM	SMPY0014001	35.5 dBm,56 %, A, dBc, dB,6x6x1.15 ,SMD ,Tri Band	
6	U602	IC	EUSY0280101	LFCSP-32 ,32 PIN,R/TP ,GSM QUAD BAND TRANSCEIVER, Othello G.	
6	VA300	VARISTOR	SEVY0005201	5.5 V, ,SMD ,1005, 50pF	
6	VA301	VARISTOR	SEVY0005201	5.5 V, ,SMD ,1005, 50pF	
6	VA303	VARISTOR	SEVY0001001	14 V, ,SMD ,50pF, 1005	
6	VA304	VARISTOR	SEVY0001001	14 V, ,SMD ,50pF, 1005	
6	VA305	VARISTOR	SEVY0001001	14 V, ,SMD ,50pF, 1005	
6	VA306	VARISTOR	SEVY0001001	14 V, ,SMD ,50pF, 1005	
6	VA307	VARISTOR	SEVY0001001	14 V, ,SMD ,50pF, 1005	
6	VA400	VARISTOR	SEVY0004101	5.6 V, ,SMD ,360pF, 1005	
6	VA401	VARISTOR	SEVY0004101	5.6 V, ,SMD ,360pF, 1005	
6	VA402	VARISTOR	SEVY0003801	18 V, ,SMD ,	
6	VA403	VARISTOR	SEVY0003801	18 V, ,SMD ,	
6	VA404	VARISTOR	SEVY0003801	18 V, ,SMD ,	
6	VA501	VARISTOR	SEVY0004101	5.6 V, ,SMD ,360pF, 1005	
6	VA502	VARISTOR	SEVY0003801	18 V, ,SMD ,	
6	VA503	VARISTOR	SEVY0003801	18 V, ,SMD ,	
6	X100	X-TAL	EXXY0018701	32.768 KHz,20 PPM,12.5 pF,70 Kohm,SMD ,3.2*1.5*0.9	
6	X200	OSCILLATOR	EXSY0022201	19.2 MHz,20 PPM,15 pF,SMD ,3.2*2.5*1.0 ,1.71V ~ 1.89V, -20'C ~ +70'C ,; ,19.2MHz ,20PPM ,1.8V ,3.2 ,2.5 ,1.0 , ,SMD ,R/TP	
6	X601	X-TAL	EXXY0024401	26 MHz,10 PPM,10 pF,.5 ohm,SMD ,32*25*0.6 ,. ,. ,. ,10PPM ,10 ,. , ,SMD ,P/TP	
6	ZD300	DIODE,TVS	EDTY0009401	VMN2 ,5 V,10 W,R/TP ,1.0*0.6*0.4 ,; , ,7.82V , , ,100mW ,[empty] ,[empty] ,2P ,1	

Level	Location No.	Description	Part number	Spec	Remark
6	ZD501	DIODE,TVS	EDTY0009401	VMN2 ,5 V,10 W,R/TP ,1.0*0.6*0.4 ,; , ,7.82V , , ,100mW ,[empty] ,[empty] ,2P ,1	
5	SAFD00	PCB ASSY,MAIN,SMT TOP	SAFD0101701		
6	C402	CAP,CERAMIC,CHIP	ECCH0004904	1 uF,6.3V ,K ,X5R ,TC ,1005 ,R/TP	
6	LD400	DIODE,LED,CHIP	EDLH0013701	WHITE ,ETC ,R/TP ,SIDEVIEW ,; ,[empty] ,2.9~3.75 ,30mA , , ,120mW ,[empty] ,[empty] ,2P	
6	LD401	DIODE,LED,CHIP	EDLH0013701	WHITE ,ETC ,R/TP ,SIDEVIEW ,; ,[empty] ,2.9~3.75 ,30mA , , ,120mW ,[empty] ,[empty] ,2P	
6	SPFY00	PCB,MAIN	SPFY0173101	FR-4 ,0.8 mm,STAGGERED-8 , ,; , , , , , , , ,	
6	U400	IC	EUSY0313401	QFN ,4 PIN,R/TP ,1.8X1.2X0.5 size wide input voltage Hall Switch	
6	VA405	VARISTOR	SEVY0004101	5.6 V, ,SMD ,360pF, 1005	_
3	SMZY00	MODULE,ETC	SMZY0014202	256MB MicroSD	

13.3 Accessory

Note: This Chapter is used for reference, Part order is ordered by SBOM standard on GCSC

Level	Location No.	Description	Part number	Spec		Remark
3	MCJA00	COVER,BATTERY	MCJA0051801	MOLD, PC LUPOY SC-1004A, , , , ,	Black	70,S
3	SBPL00	BATTERY PACK,LI-ION	SBPL0092901	3.7 V,800 mAh,1 CELL,PRISMATIC ,KM500 Latin America BATT, Pb-Free ,; ,3.7 ,800 ,0.2C ,PRISMATIC ,50x34x36 , ,BLACK ,Innerpack ,Latin America Label	Black	69
3	SGDY00	DATA CABLE	SGDY0010904	; ,[empty] ,[empty] ,[empty] ,18 ,BLACK ,6.2mm Plug Datacable ,[empty]		
3	SGEY00	EAR PHONE/EAR MIKE SET	SGEY0005537			
3	SSAD00	ADAPTOR,AC-DC	SSAD0024601	100-240V ,5060 Hz,5.1 V,.7 A,NOM ,AC-DC ADAPTOR ,; ,85Vac~264Vac ,5.1V +0.15V, -0.2V ,700mA ,5060 , ,WALL 2P ,I/O CONNECTOR ,		
		ADAPTOR,AC-DC	SSAD0024602	100-240V ,5060 Hz,5.1 V,.7 A,NOM ,AC-DC ADAPTOR ,; ,85Vac~264Vac ,5.1V (+0.15V, -0.2V) ,700mA ,5060 , ,WALL 2P ,I/O CONNECTOR ,		